

1	Cover Sheet
2	Block Diagram
3	Clock Distribution
4	CPU-CLK/Control/MISC/PEG
5	CPU-Memory
6	CPU-Power
7	CPU-GND
8	DDR III DIMM 3 / DIMM 1
9	DDR III DIMM 4 / DIMM 2
10	PCH-PCIE/DMI/USB/CLK
11	PCH-SATA/HOST/GPIO/DDI/VGA
12	PCH-SMB/LPC/AUDIO/RTC
13	PCH-Power
14	PCH-GND
15	PCIE x16 and x1 Slots
16	Mini PCIE/Mini SATA
17	SATA
18	HDMI/DVI
19	D-SUB
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21	Rear USB Connectors
22	USB Power / iCharger
23	Audio Codec-ALC887-VD
24	Gigabit Intel Clarkville-V I217
25	SIO F71889AD
26	FAN/PS2/COM/LPT
27	ATX PWR/FRTP/LED/Buzzer/EMI/APS
28	ACPI
29	DDR Power
30	PCH & ME Core Power
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32	VCCP
33	CPU/PCH XDP
34	Manual & Option Parts
37	Reset/Pwrok/PON
38	Power Map
39	GPIO Table
40	History

# MS-7852

Version : 1.0  
uATX (244mm x 244mm)

## CPU :

**Intel Haswell Processor**

## System Chipset :

**Intel Lynx Point Chipset**

## On Board Chipset :

**VRM 12.5 --ISL95816HRZ 4 Phase (95W)**

**Gigabit Intel Clarkville-V I217**

**HDA Codec -- Realtek ALC887**

**Super I/O -- F71889AD**

**SPI Flash 64Mb**

## Main Memory :

**2 Channel DDR III \* 4 (Max 32GB)**

## Expansion Slot :

**PCI Express x16 Slot \* 1**

**PCI Express x1 Slot \* 3**

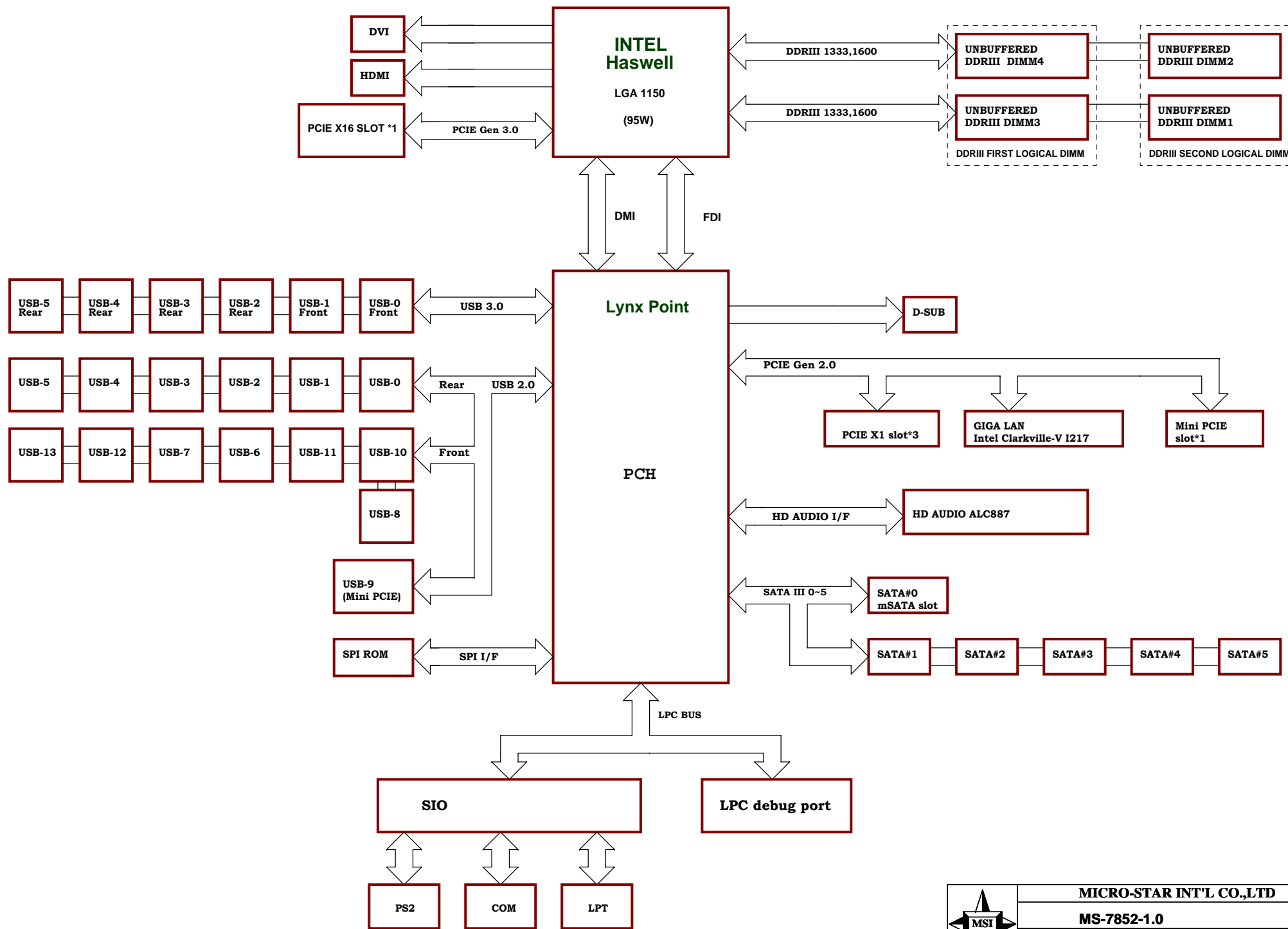
**Mini PCIESlot \* 1**

**Mini SATA Slot \* 1**



MICRO-STAR INT'L CO.,LTD			
MS-7852-1.0			
Size Custom	Document Description <b>Cover Sheet</b>		Rev <b>1.0</b>
Date: Wednesday, March 27, 2013		Sheet 1	of 40







PROCESSOR

DMI 100MHz

DP 135MHz

PCH

PCIE GENIII 100MHz

PCIE x16 SLOT

PCIE GENII 100MHz

PCIE x1 SLOT

PCIE GENII 100MHz

Mini PCIE x1 SLOT

PCIE GENII 100MHz

LAN

PCI 33MHz

LPC DEBUG

PCI 33MHz

SIO

PCI 33MHz

loopback

PCI 33MHz

TPM



MICRO-STAR INT'L CO.,LTD

MS-7852-1.0

Size  
Custom

Document Description  
Clock Distribution

Rev  
1.0

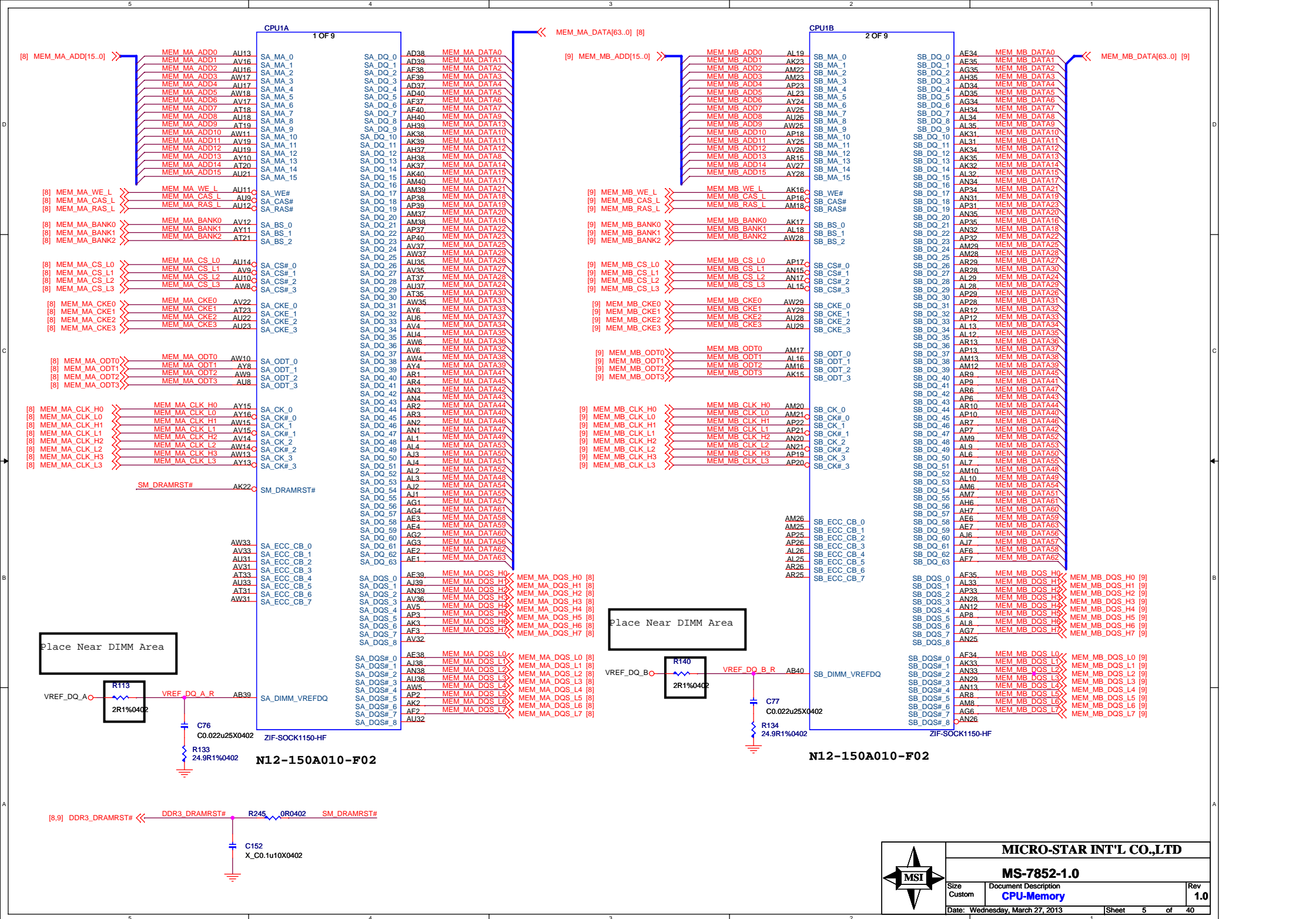
Date: Wednesday, March 27, 2013

Sheet 3 of 40

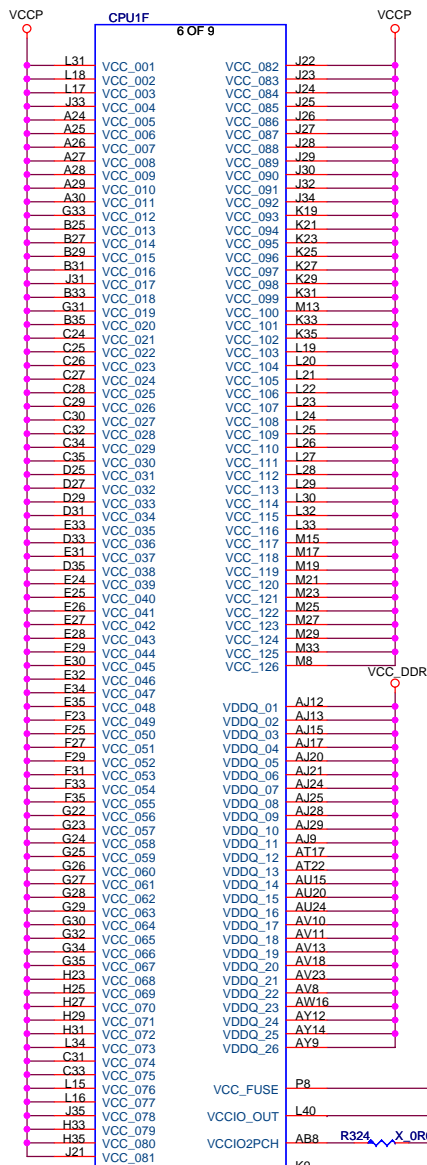


Date: Wednesday, March 27, 2013      Sheet 4 of 40





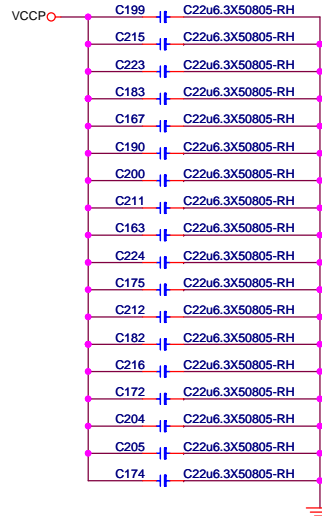




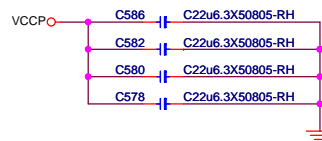
ZIF-SOCK1150-HF  
**N12-150A010-F02**

### VCCP-Decoupling

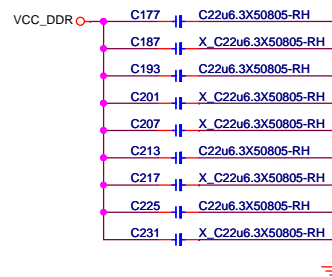
PLACE THESE CAPS INSIDE CPU SOCKET CAVITY



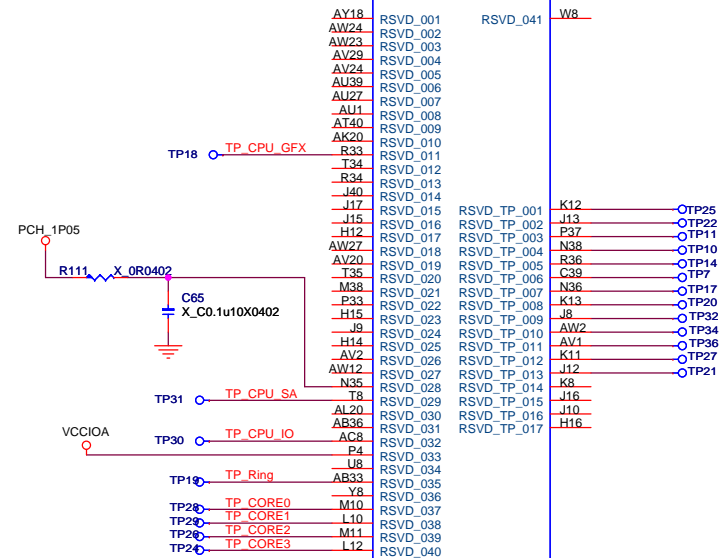
PLACE THESE CAPS NEAR CPU SOCKET EDGE



### VCC\_DDR-Decoupling near to CPU



CPU1I  
9 OF 9

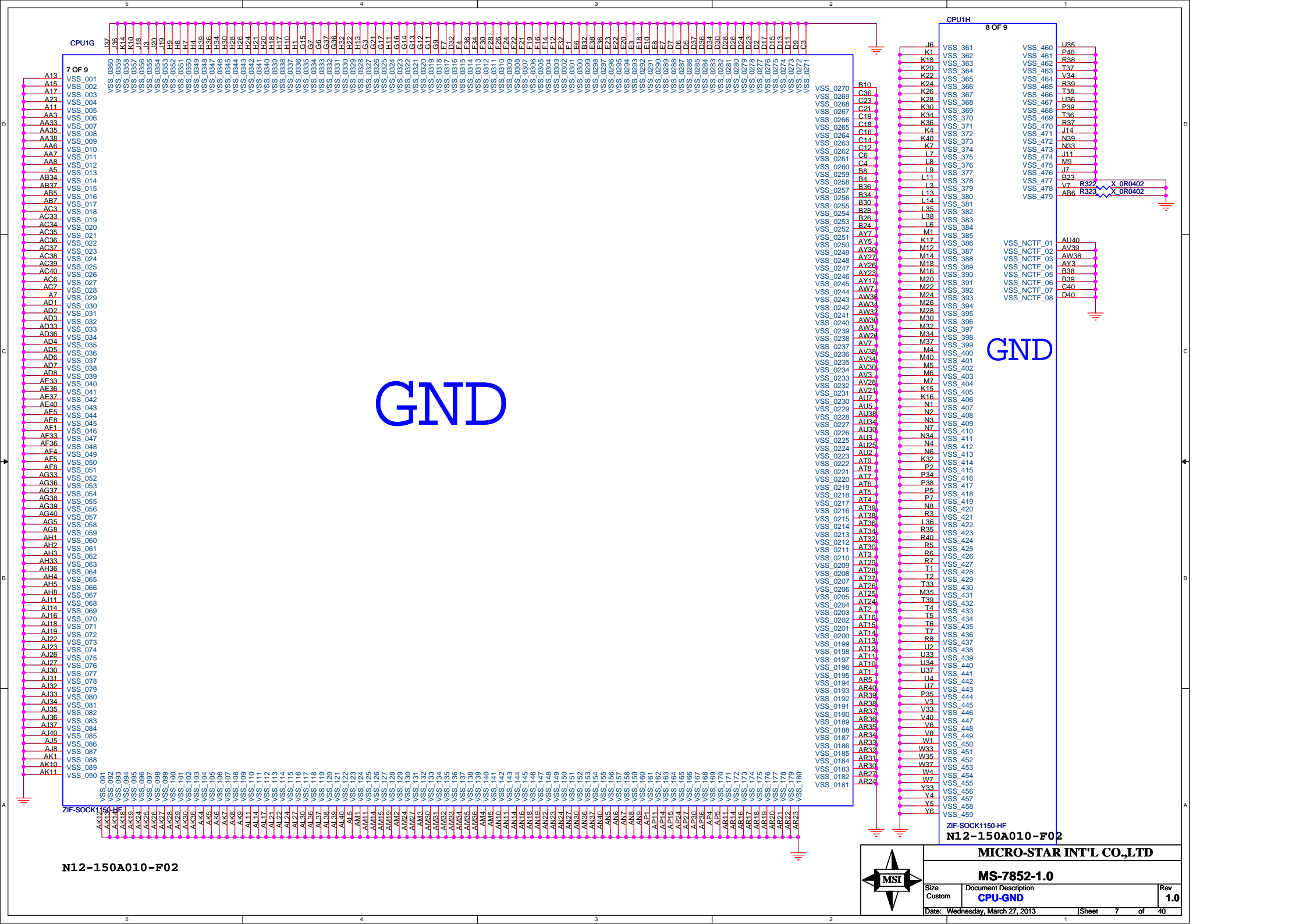


**MICRO-STAR INT'L CO.,LTD**

**MS-7852-1.0**

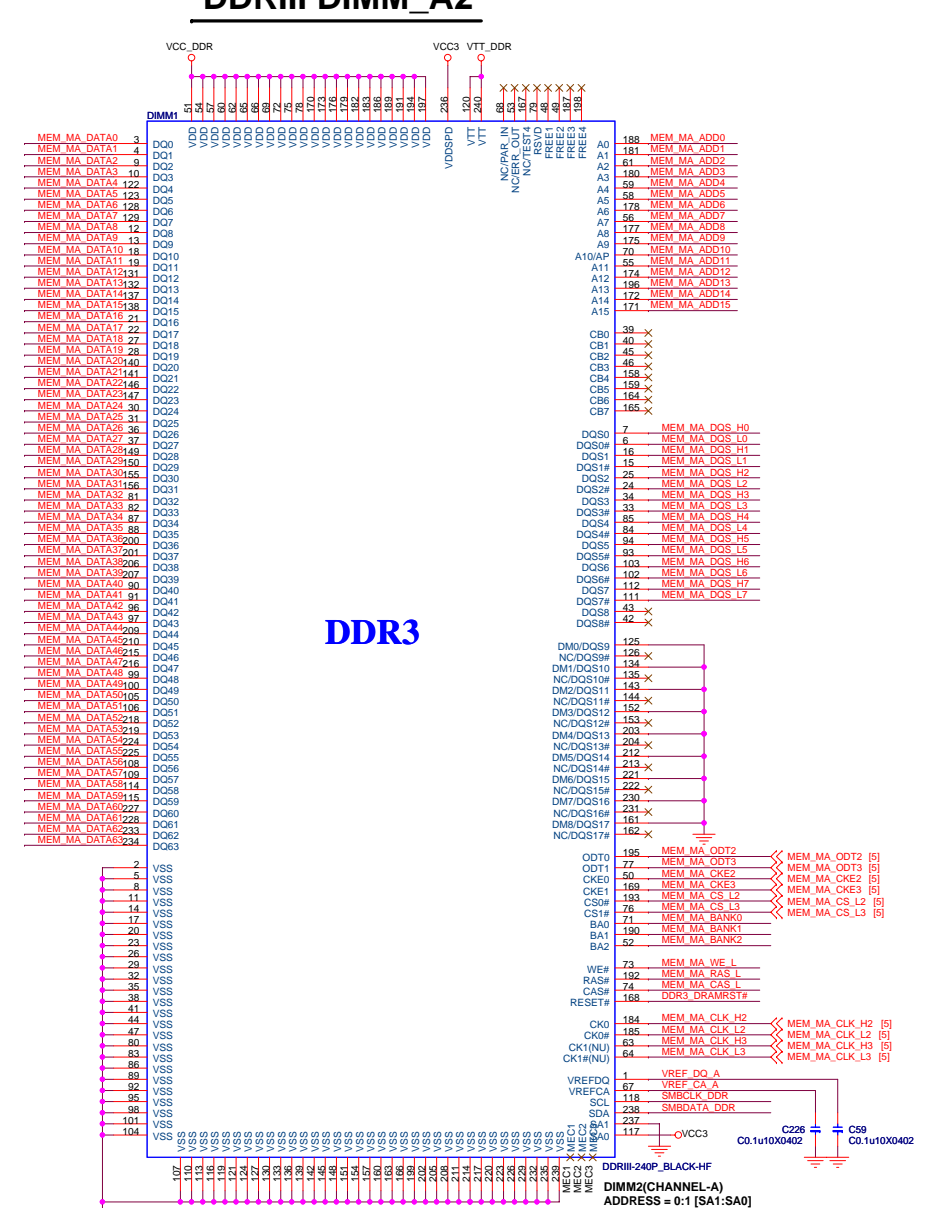
Size	Document Description	Rev
Custom	CPU-Power	1.0
Date: Wednesday, March 27, 2013		
Sheet 6 of 40		







## DDRIII DIMM\_A2

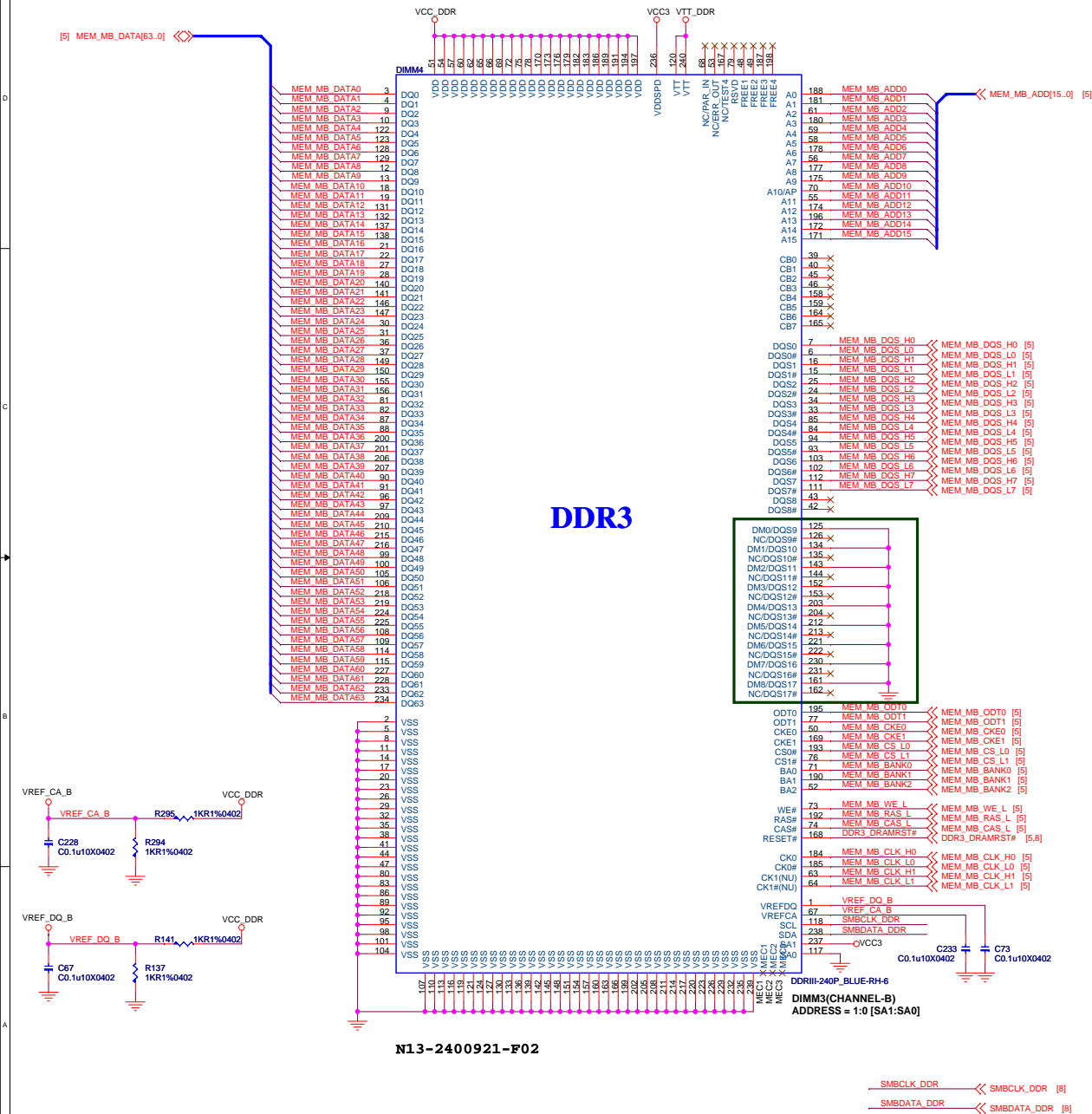


**N13-2401081-F02**

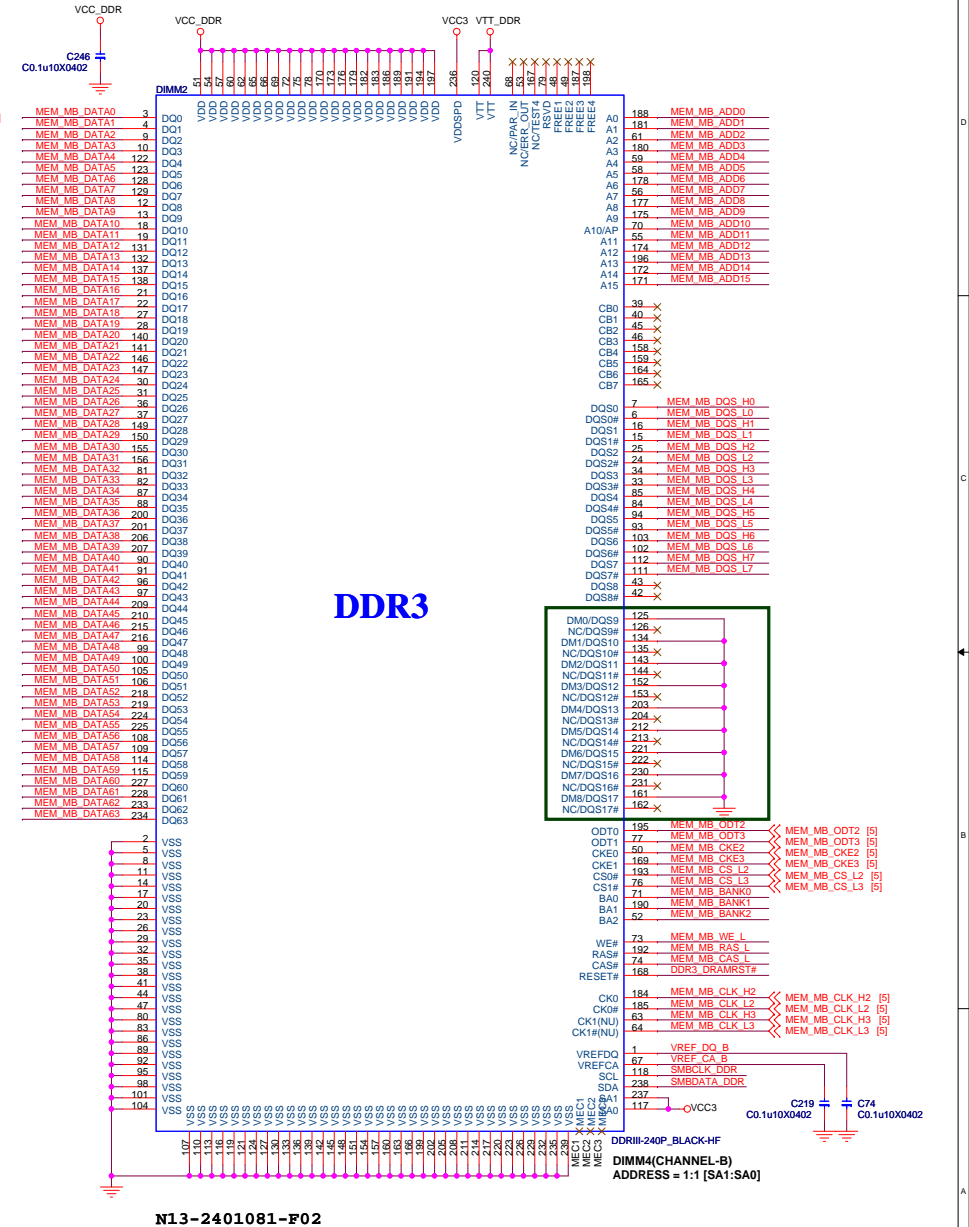




## DDRIII DIMM\_B1



## DDRIII DIMM\_B2



**N13-2400921-F02**

**N13-2401081-F02**

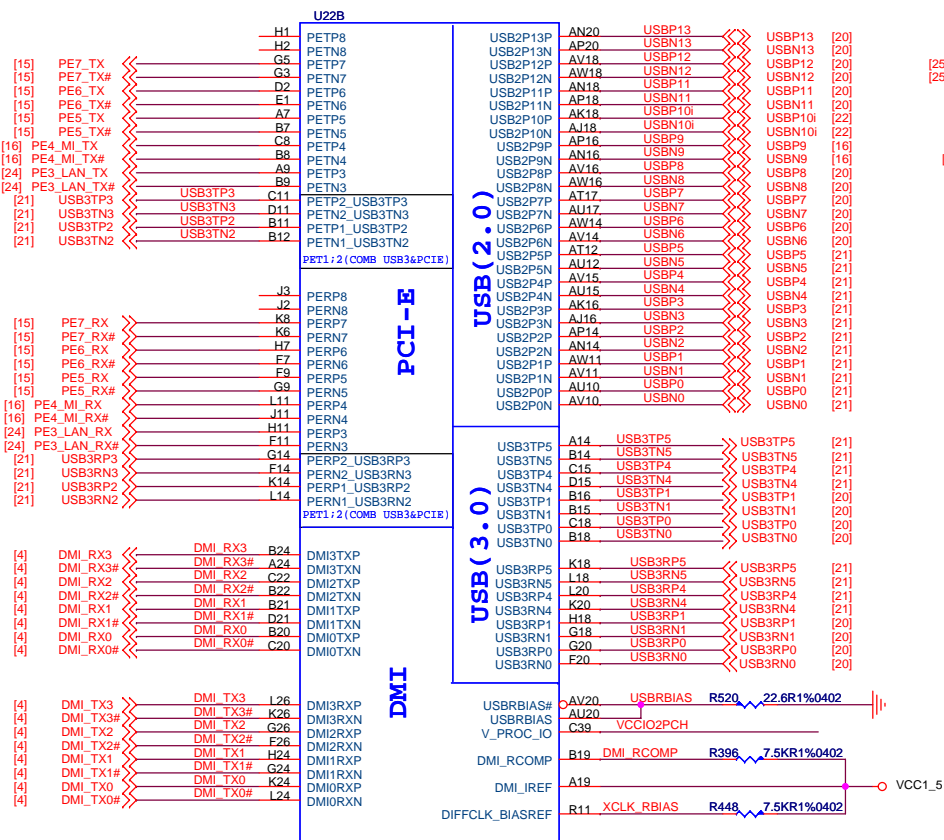


**MICRO-STAR INT'L CO.,LTD**

MS-7852-1.0

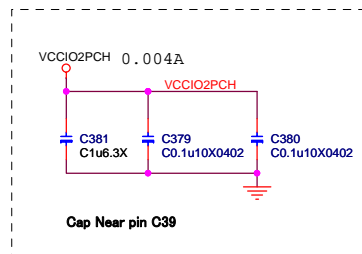
Size Custom	Document Description <b>DDR III DIMM 3 / DIMM 4</b>	Rev <b>1.0</b>
Date: Wednesday, March 27, 2013		Sheet 9 of 40



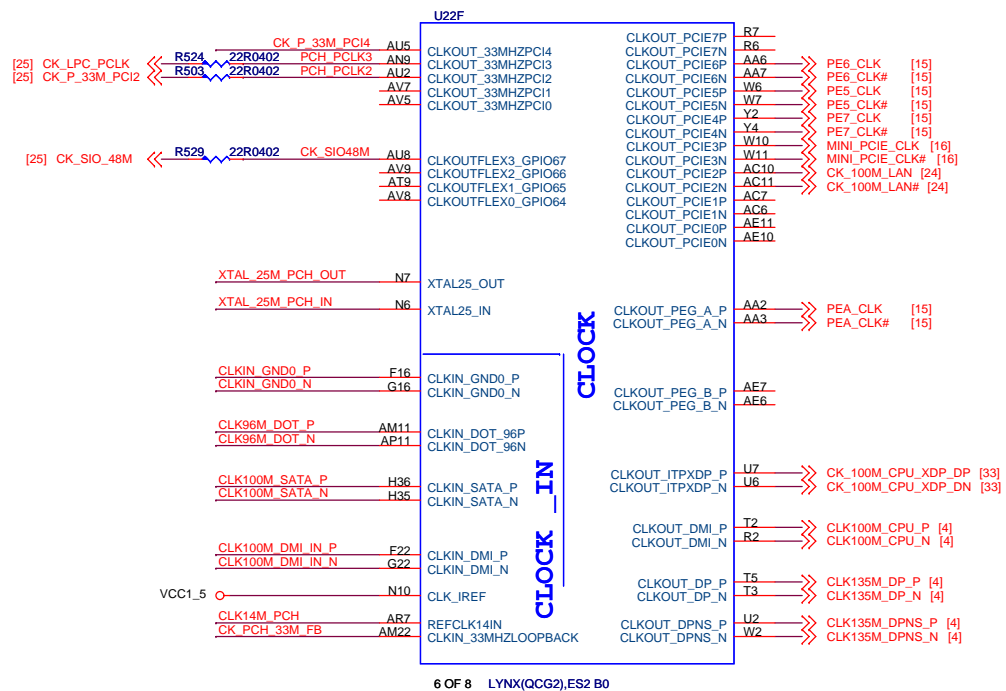
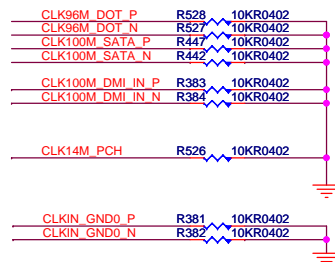


LYNX(QCG2),ES2FB8

**OB1-7837001**



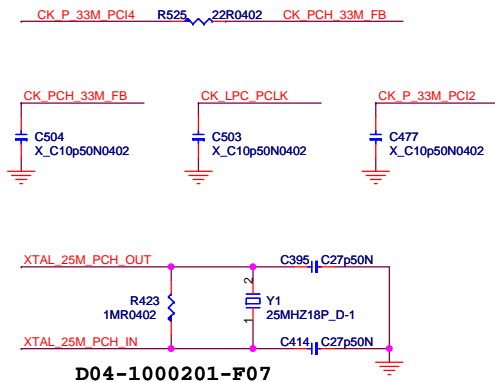
no clock gen pull down



6 OF 8 LYNX(QCG2),ES2 B0

**OB1-7837001**

## PCICLK LOOPBACK



**MICRO-STAR INT'L CO.,LTD**

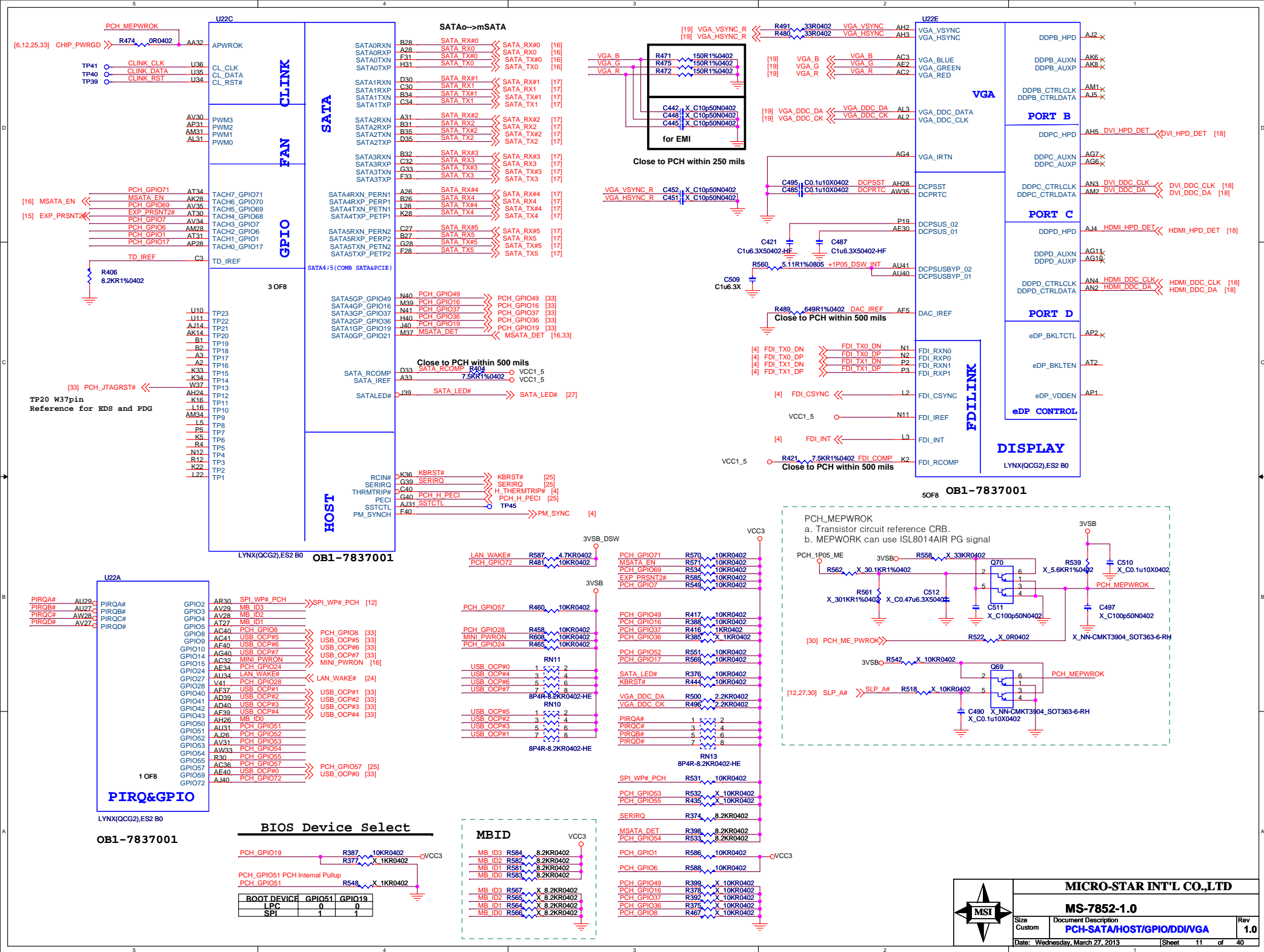
**MS-7852-1.0**

Size	Document Description
Custom	<b>PCH-PCIE/DMI/USB/CLK</b>

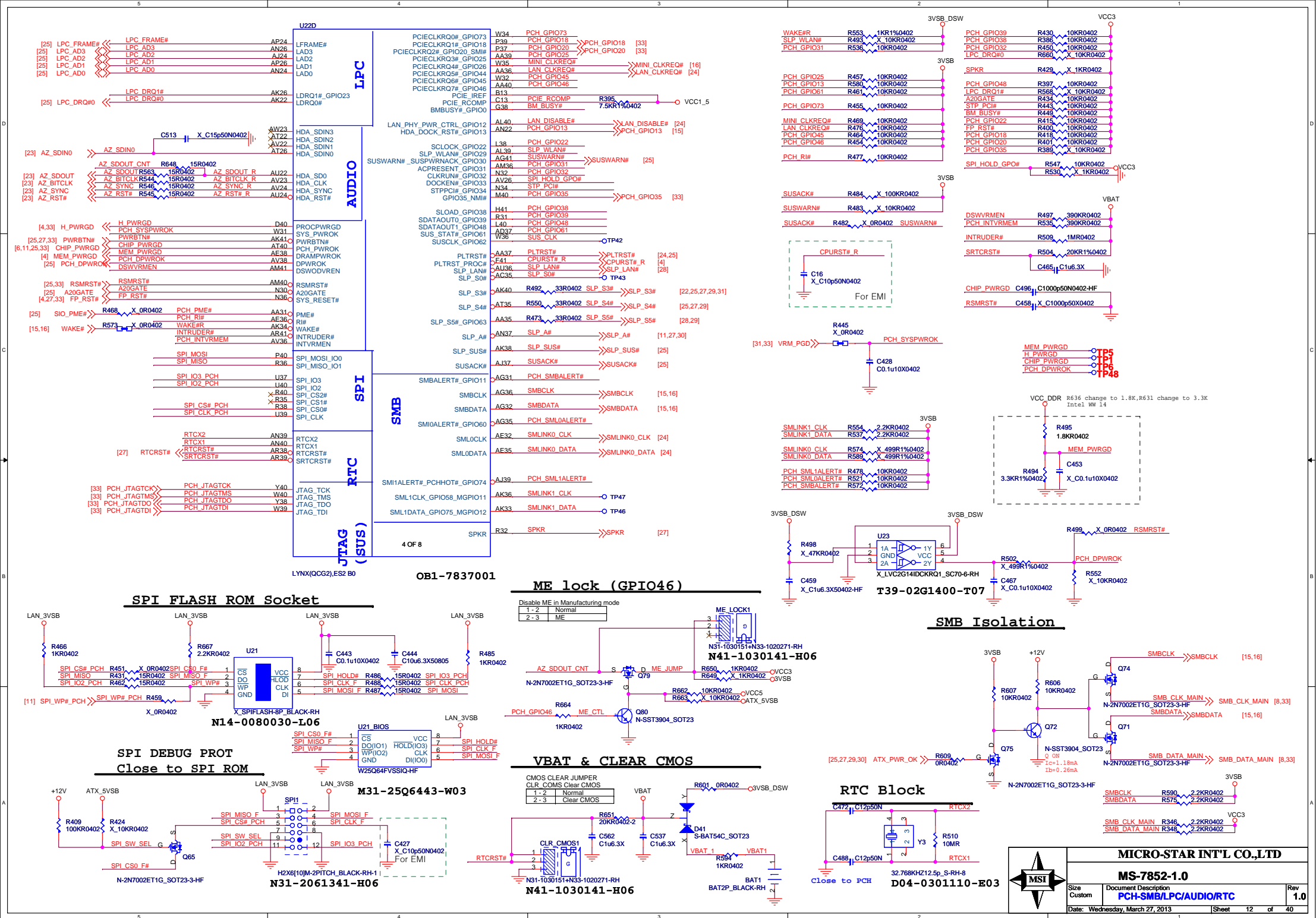
Rev	
1.0	

Date: Wednesday, March 27, 2013	Sheet 10 of 40
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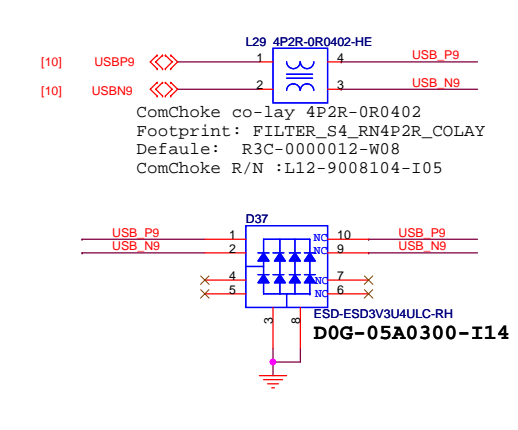
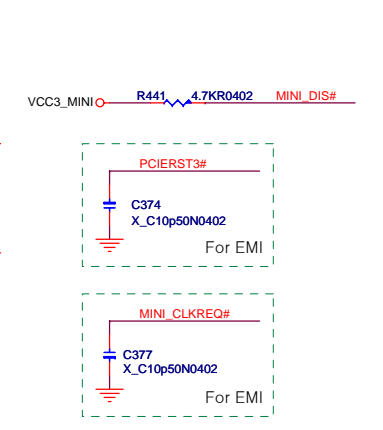
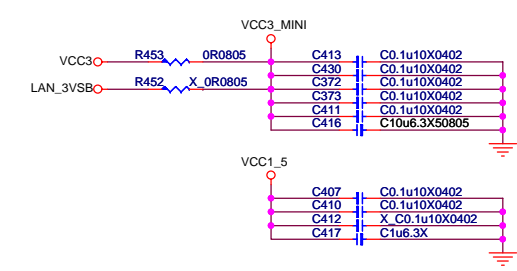
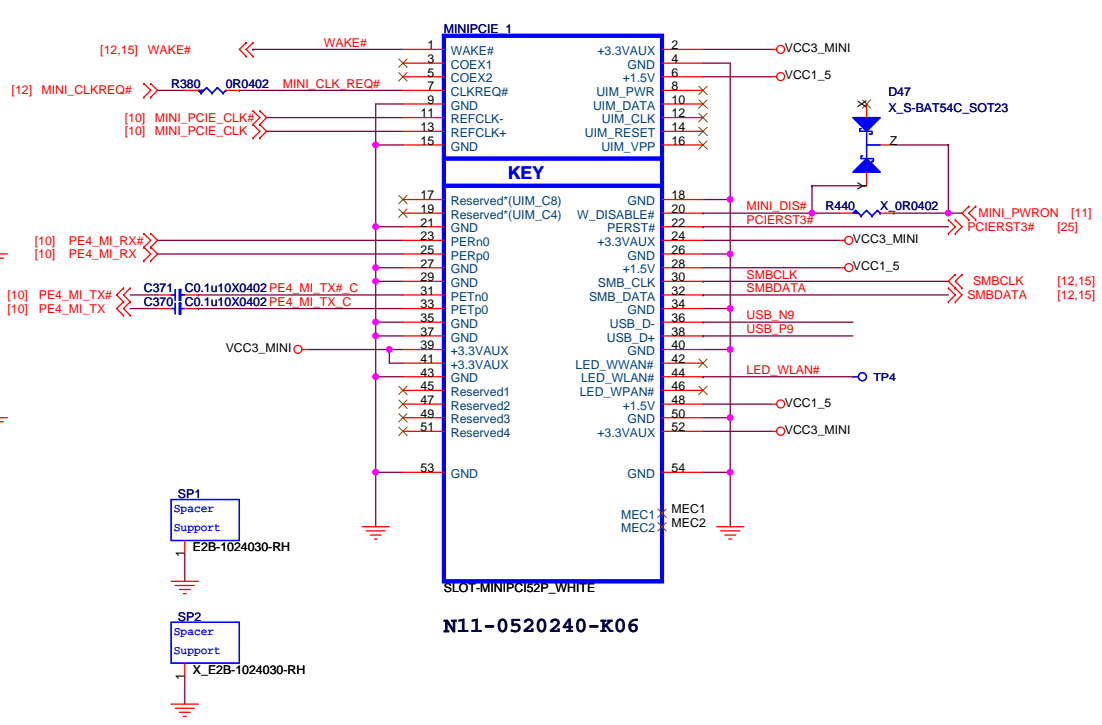
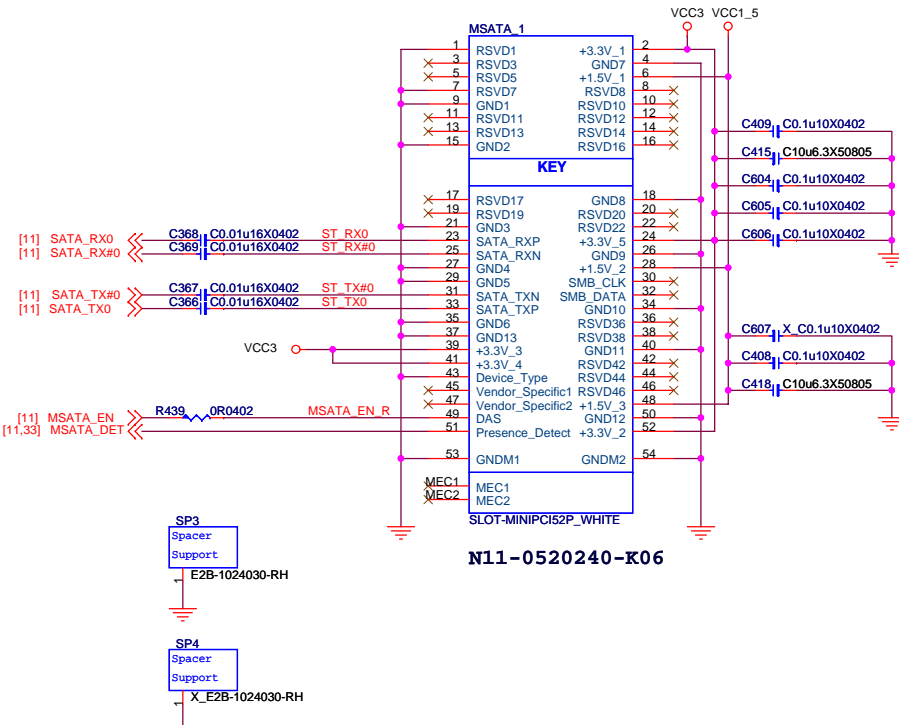
# PCI EXPRESS X16 SLOT





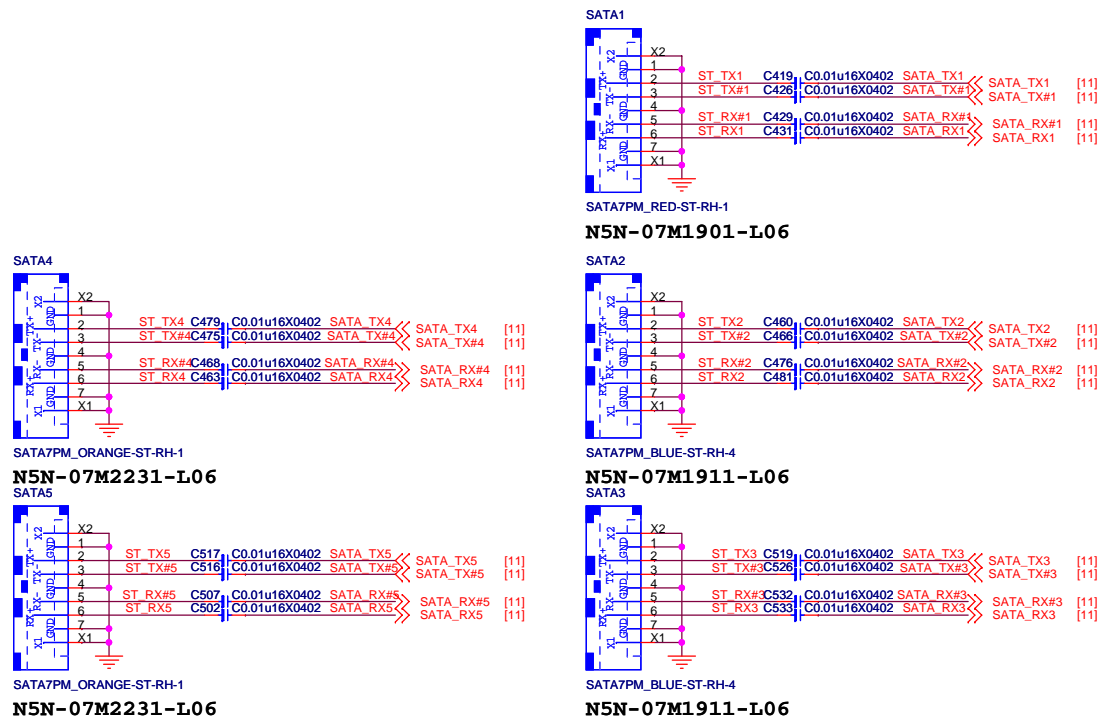
## Full-size Mini SATA Card

## Half-size Mini PCIE Card





# SATA connector



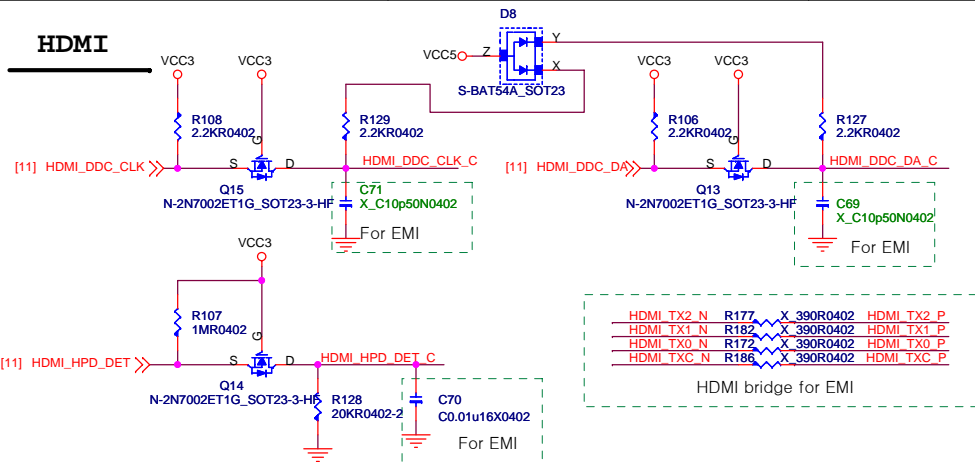
SATA Master / Slave CFG	
	Red Primary Master (Port 1)
Orange Primary Master (Port 4)	Light Blue Secondary Master (Port 2)
Orange Secondary Slave (Port 5)	Light Blue Secondary Master (Port 3)

SATA#0	Primary Master
SATA#1	Secondary Master
SATA#2	Primary Slave
SATA#3	Secondary Slave
SATA#4	Primary Master
SATA#5	Secondary Master

ROUTE TRACE LENGTH NO LONGER THAN 450 MILS TO RESISTOR

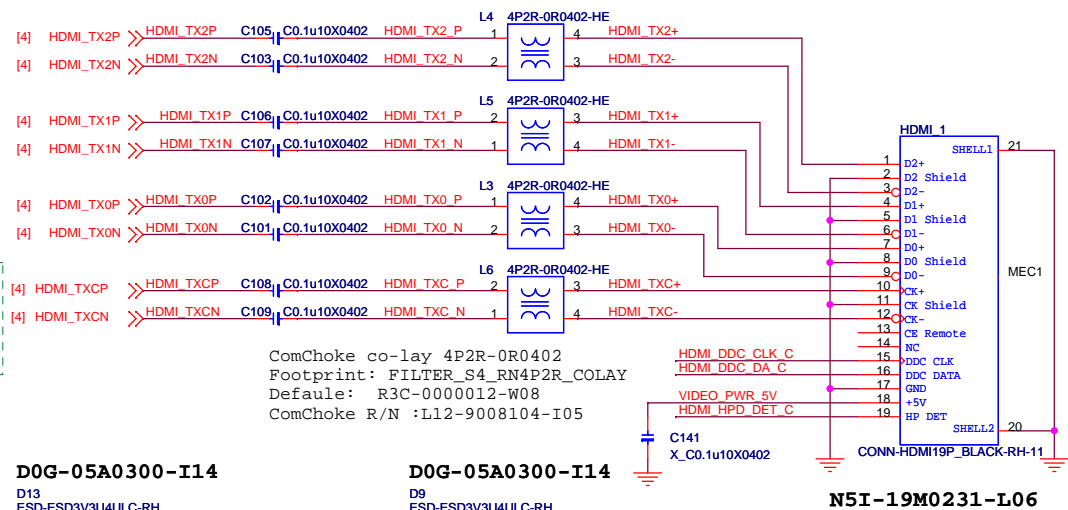


# HDMI



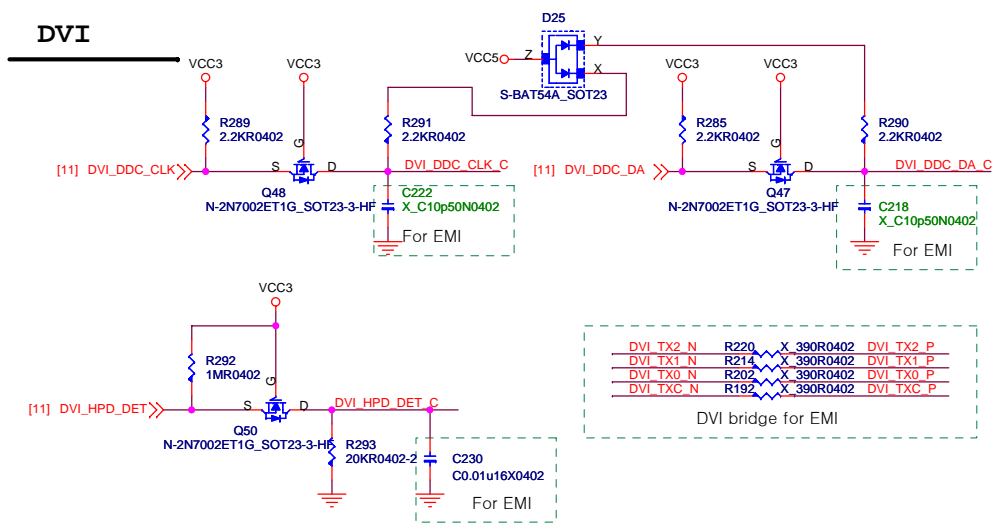
HDMI bridge for EMI

HDMI TX2_N	R177	X	390R0402	HDMI TX2_P
HDMI TX1_N	R182	X	390R0402	HDMI TX1_P
HDMI TX0_N	R172	X	390R0402	HDMI TX0_P
HDMI TXC_N	R186	X	390R0402	HDMI TXC_P



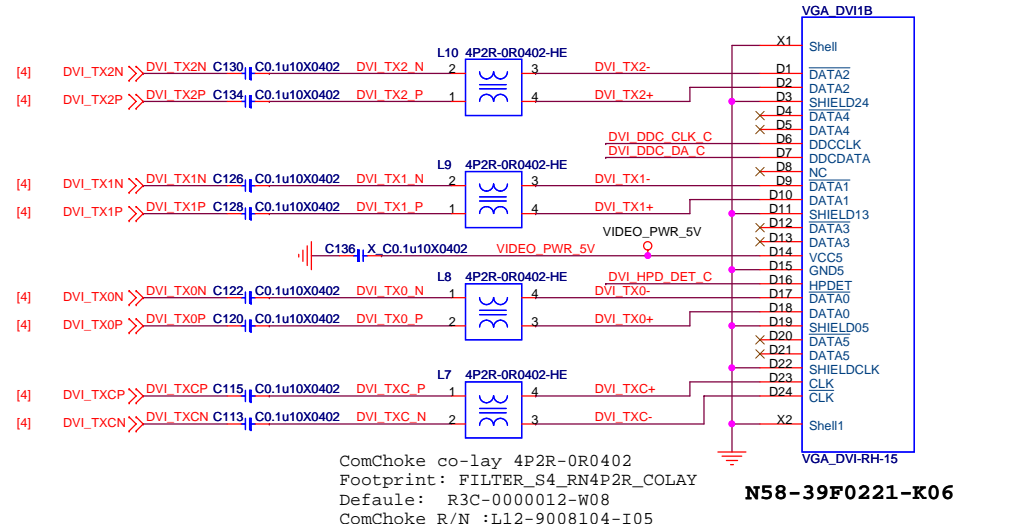
ComChoke co-lay 4P2R-0R0402  
Footprint: FILTER\_S4\_RN4P2R\_COLAY  
Defaule: R3C-0000012-W08  
ComChoke R/N :L12-9008104-I05

# DVI

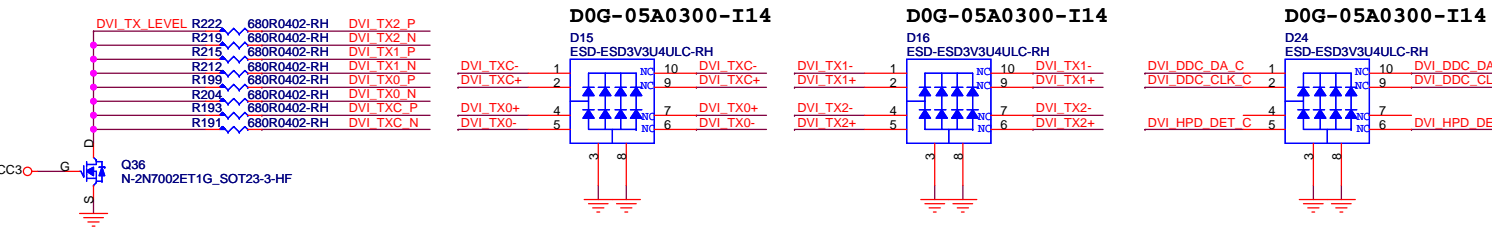


DVI bridge for EMI

DVI TX2_N	R220	X	390R0402	DVI TX2_P
DVI TX1_N	R214	X	390R0402	DVI TX1_P
DVI TX0_N	R202	X	390R0402	DVI TX0_P
DVI TXC_N	R192	X	390R0402	DVI TXC_P

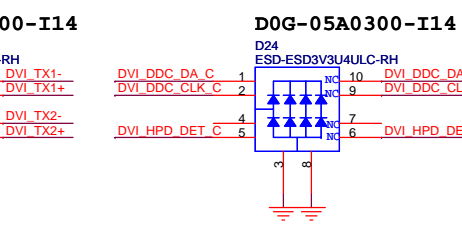


ComChoke co-lay 4P2R-0R0402  
Footprint: FILTER\_S4\_RN4P2R\_COLAY  
Defaule: R3C-0000012-W08  
ComChoke R/N :L12-9008104-I05



DVI bridge for EMI

DVI TX2_N	R220	X	390R0402	DVI TX2_P
DVI TX1_N	R214	X	390R0402	DVI TX1_P
DVI TX0_N	R202	X	390R0402	DVI TX0_P
DVI TXC_N	R192	X	390R0402	DVI TXC_P



DVI bridge for EMI

DVI TX2_N	R220	X	390R0402	DVI TX2_P
DVI TX1_N	R214	X	390R0402	DVI TX1_P
DVI TX0_N	R202	X	390R0402	DVI TX0_P
DVI TXC_N	R192	X	390R0402	DVI TXC_P



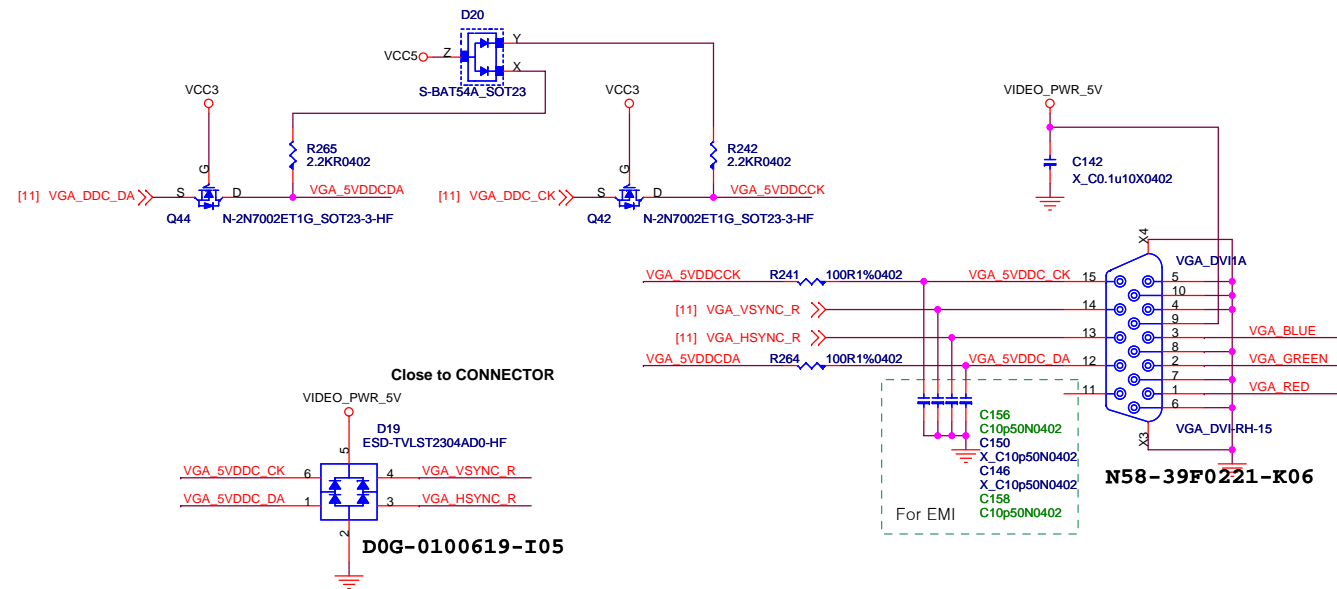
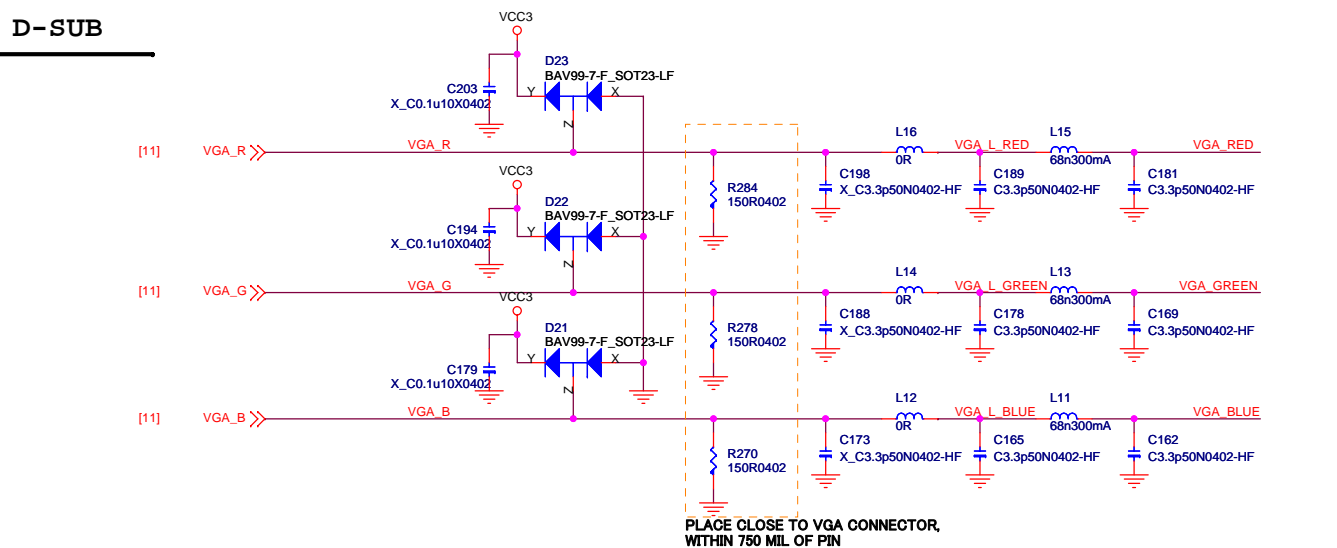
MICRO-STAR INT'L CO.,LTD

MS-7852-1.0

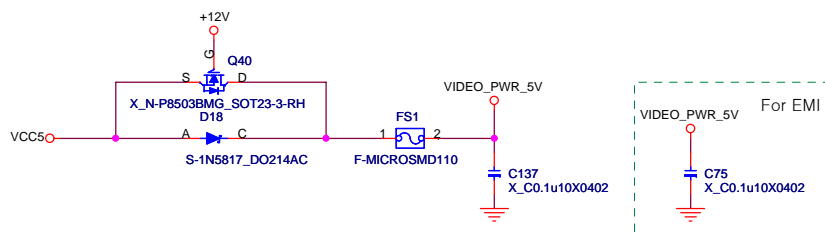
Size	Document Description	Rev
Custom	HDMI/DVI	1.0
Date: Wednesday, March 27, 2013	Sheet 18 of 40	



# D-SUB



## VIDEO\_PWR\_5V



MICRO-STAR INT'L CO.,LTD

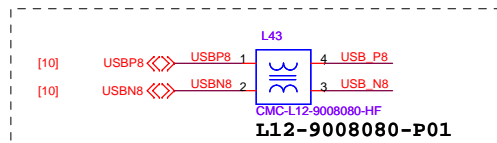
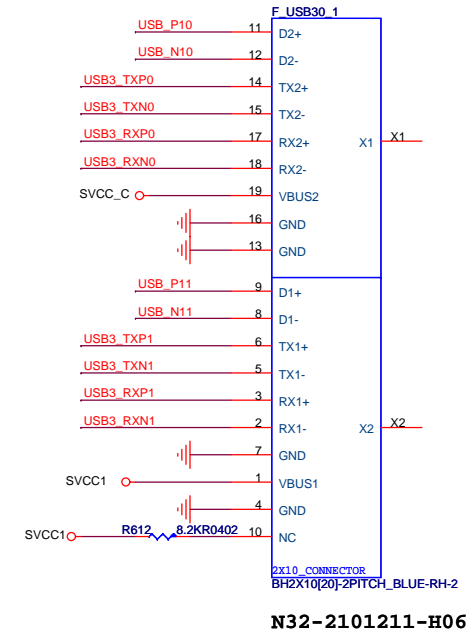
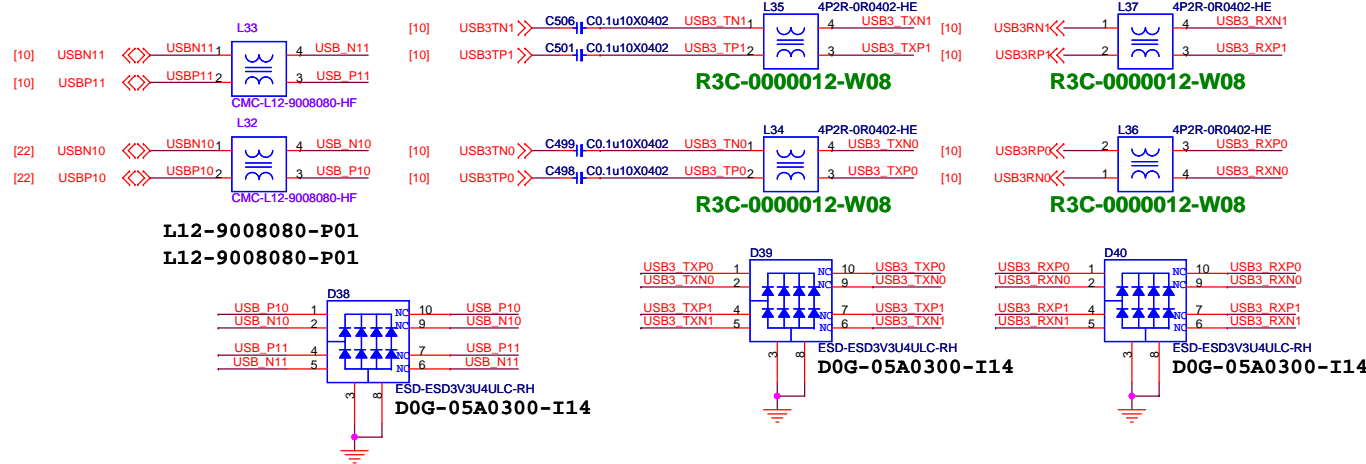
MS-7852-1.0

Size	Document Description	Rev
Custom	D-SUB	1.0
Date:	Wednesday, March 27, 2013	Sheet 19 of 40

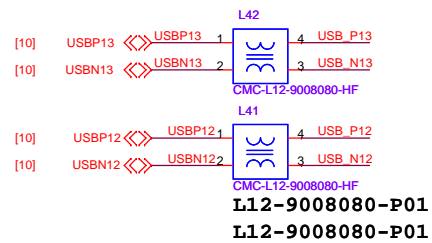
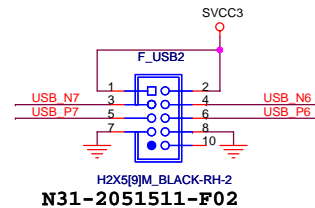
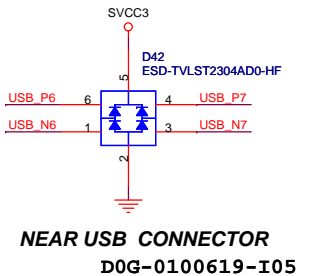
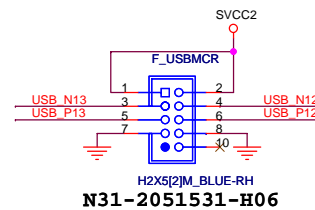
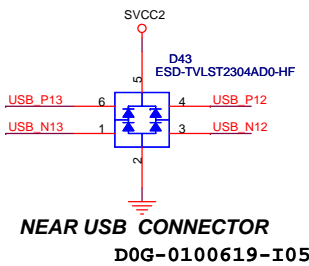
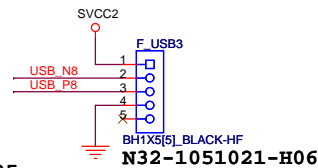
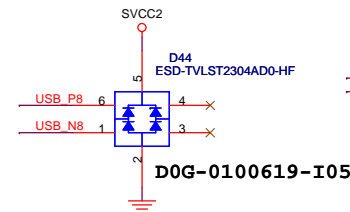


# **FRONT PANEL USB 3.0 PORT 0,1 and USB2.0 PORT 10,11**

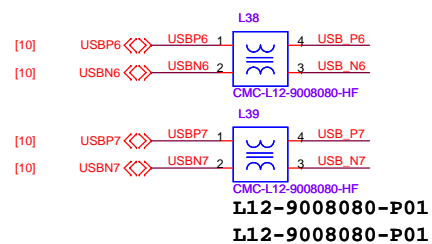
The same footprint  
CMC PN : L12-9008080-P01  
0 ohm PN : R3C-0000012-W08



## **FRONT PANEL USB2.0 CON for USB PORT 8**



## **FRONT PANEL USB2.0 CON for USB PORT 7,12**

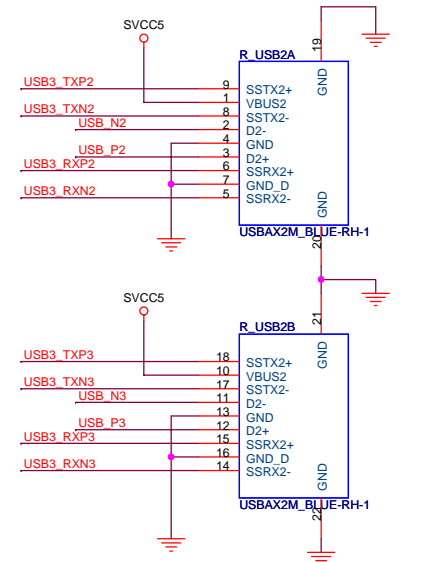
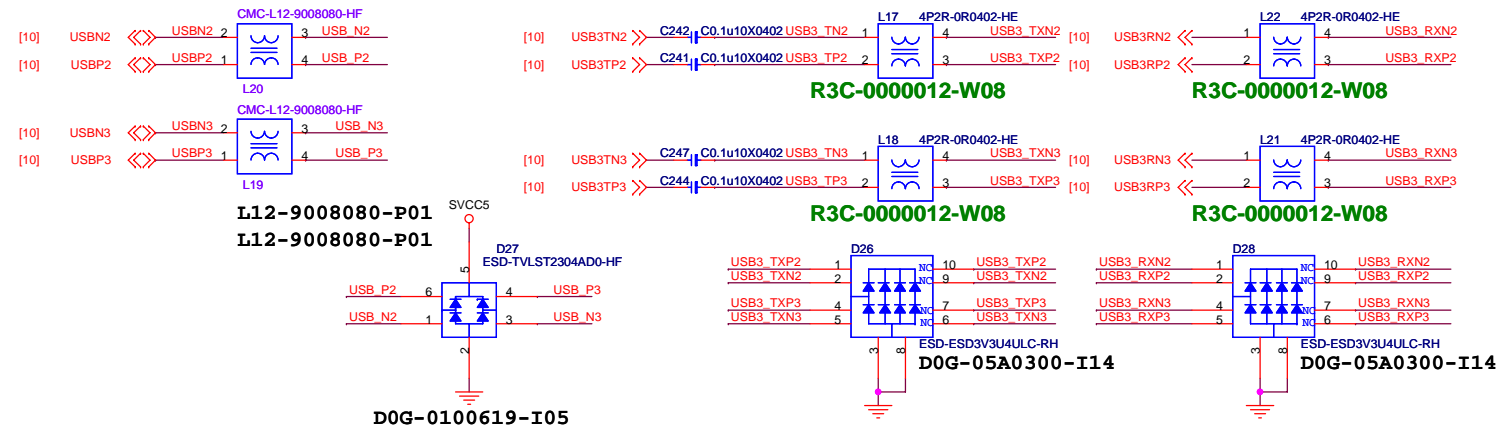


MICRO-STAR INT'L CO.,LTD		
MS-7852-1.0		
Size Custom	Document Description <b>Front USB port</b>	Rev 1.0
Date: Wednesday, March 27, 2013	Sheet 20	of 40



### REAR PANEL USB 3.0 PORT 2,3 and USB2.0 PORT 2,3

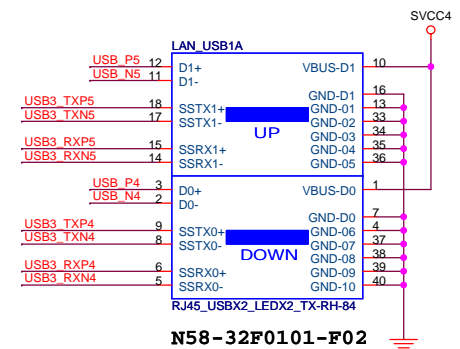
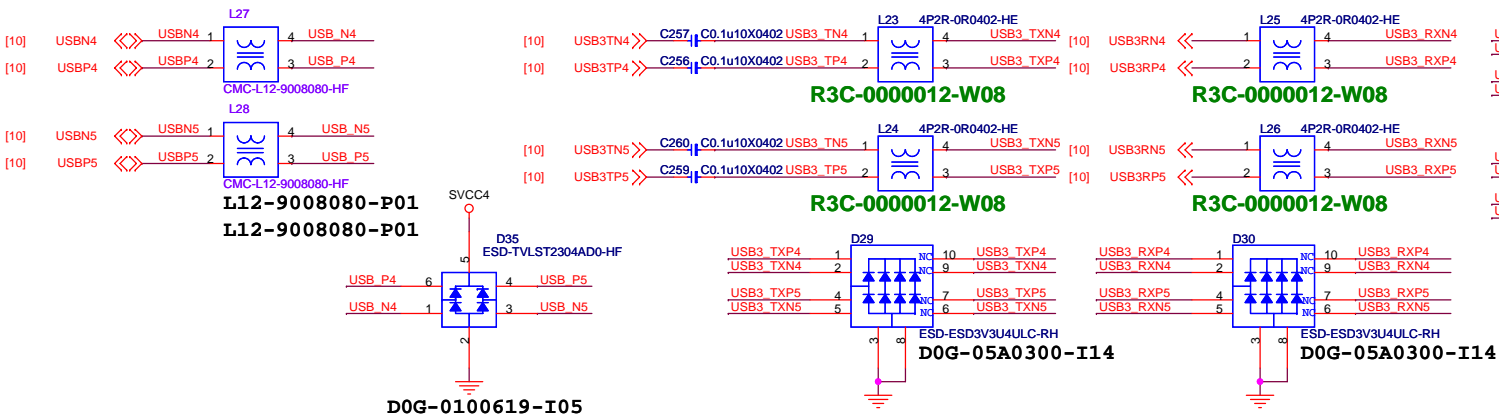
The same footprint  
CMC PN : L12-9008080-P01  
0 ohm PN : R3C-0000012-W08



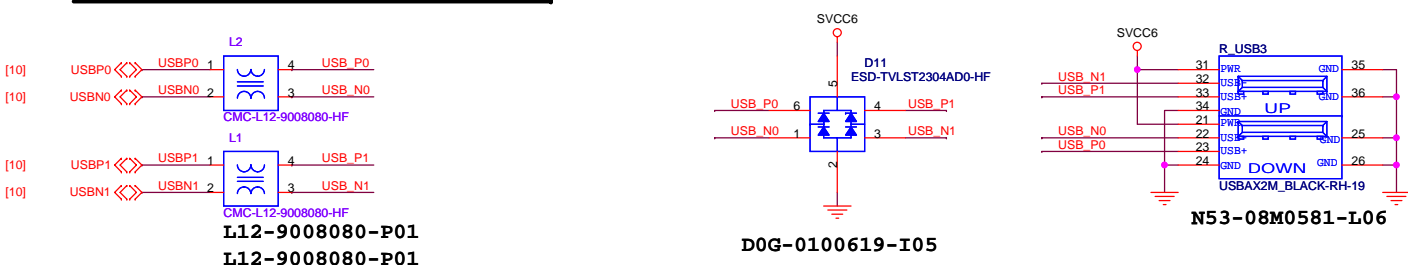
N53-18M0021-F02  
N53-18M0021-F02

### **REAR PANEL USB 3.0 PORT 4,5 and USB2.0 PORT 4,5**

The same footprint  
CMC PN : L12-9008080-P01  
0 ohm PN : R3C-0000012-W08



**REAR PANEL USB2.0 CON for USB PORT 0,1**



**MICRO-STAR INT'L CO.,LTD**

MS-7852-1.0

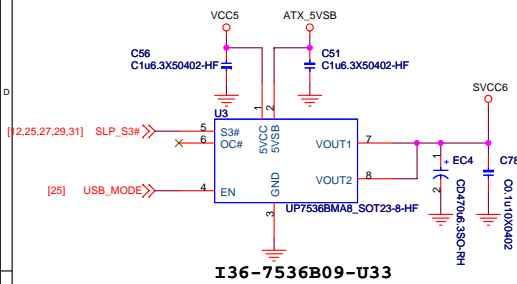
Size Custom	Document Description <b>Rear USB port</b>
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Rev	
<b>1.0</b>	

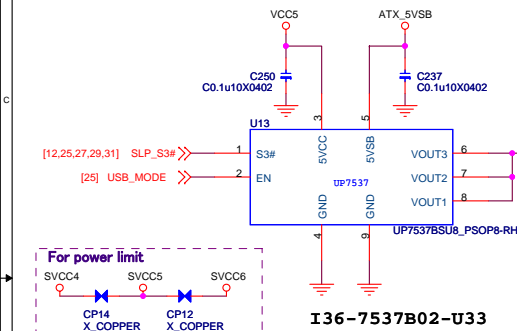


## Power Circuit for Rear USB

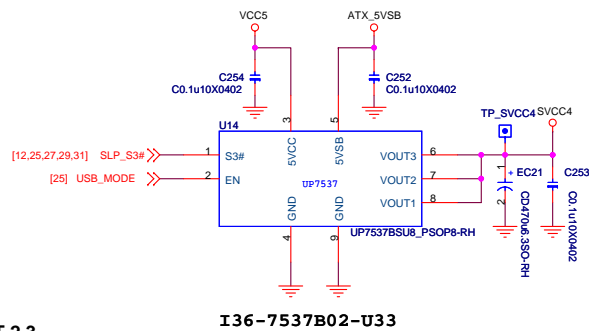
**USB3 : USB2.0 CON for USB PORT 0,1**



**USB2 : USB 3.0 PORT 2,3 and USB2.0 PORT 2,3**

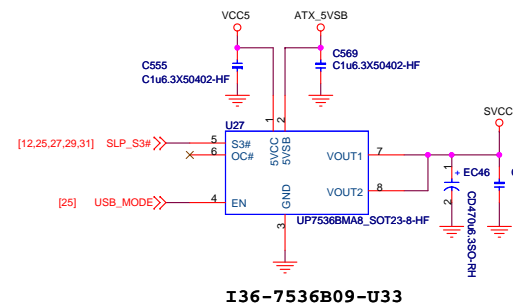


**LAN\_USB1A : USB 3.0 PORT 2,3 and USB2.0 PORT 2,3**

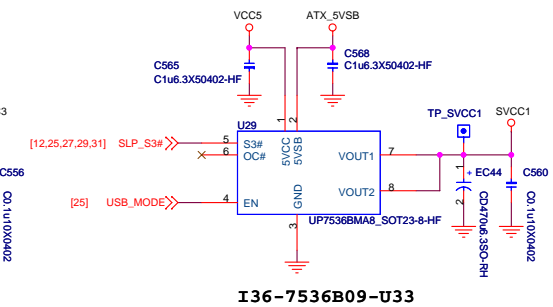


## Power Circuit for Front USB

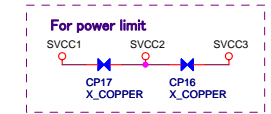
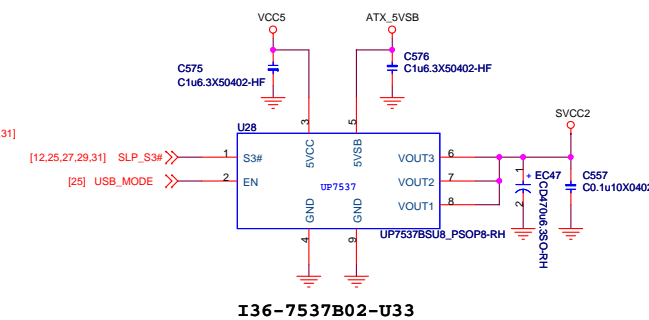
**JUSBF2, JUSB1 : USB2.0 CON for USB PORT 7,12**



**JUSBF1 : USB 3.0 PORT 1 and USB2.0 PORT 11**

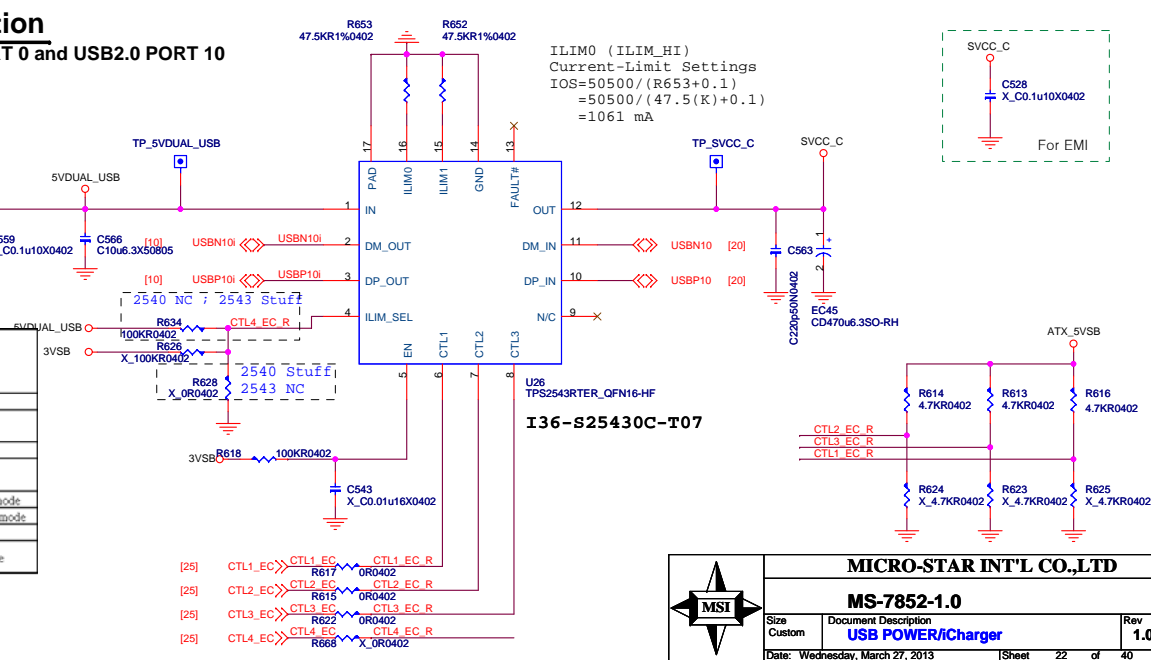
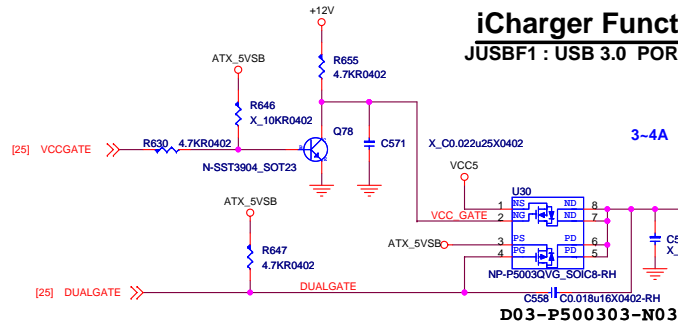


**JUSBMCR : USB2.0 CON for USB PORT 6,8**



## iCharger Function

**JUSBF1 : USB 3.0 PORT 0 and USB2.0 PORT 10**



CTL1	CTL2	CTL3	ILIM_SEL	SYSTEM GLOBAL POWER STATE	TFS2543 CHARGING MODE	CURRENT LIMIT SETTING	STATUS OUTPUT (Active low)	COMMENT
0	0	0	1		Discharge	NA	OFF	OUT held low
0	0	1	1	S4/S5	DCF_Auto mode, load detection with power wake thresholds	IOS_FW & ILIM_HI <sup>(3)</sup>	DCF load present <sup>(3)</sup>	Data Lines Disconnected and Load Detect Function Active
0	1	0	1	S3	SDF, keyboard/mouse wake-up	ILIM_HI	OFF	Data Lines connected
0	1	1	1	S3	DCF_Auto mode, keyboard/mouse wake-up, load detection with ILIM_LO + 60mA thresholds	ILIM_HI	DCF load present <sup>(3)</sup>	Data Lines Disconnected and Load Detect Function Active
1	0	0	1		DCF_Shorted	ILIM_HI	OFF	Device Forced to stay in DCF BC 1.2 charging mode
1	0	1	1		DCF	ILIM_HI	OFF	Device Forced to stay in DCF Divider 1 charging mode
1	1	0	1	S0	SDF	ILIM_HI	OFF	Data Lines Connected
1	1	1	1	S0	CDP(4), Load detect with ILIM_LO + 60mA thresholds or if a RCL1.2 primary detection occurs	ILIM_HI	DCF load present <sup>(3)</sup>	Data Lines Connected and Load Detect Active

(1) TP52543 : Current limit (IOS) is automatically switched between IOS\_FW and the value set by ILIM\_HI according to the Load Detect - Power Wake functionality.



**MICRO-STAR INT'L CO.,LTD**

**MS-7852-1.0**

Size Custom	Document Description <b>USB POWER/iCharger</b>	Rev <b>1.0</b>
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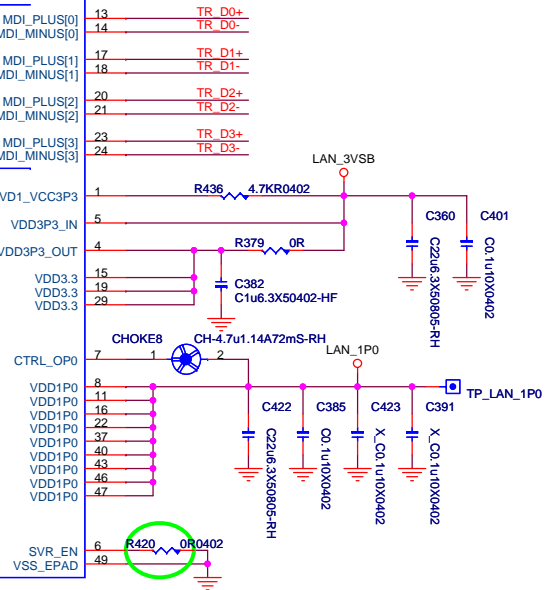




The image contains three schematic diagrams:

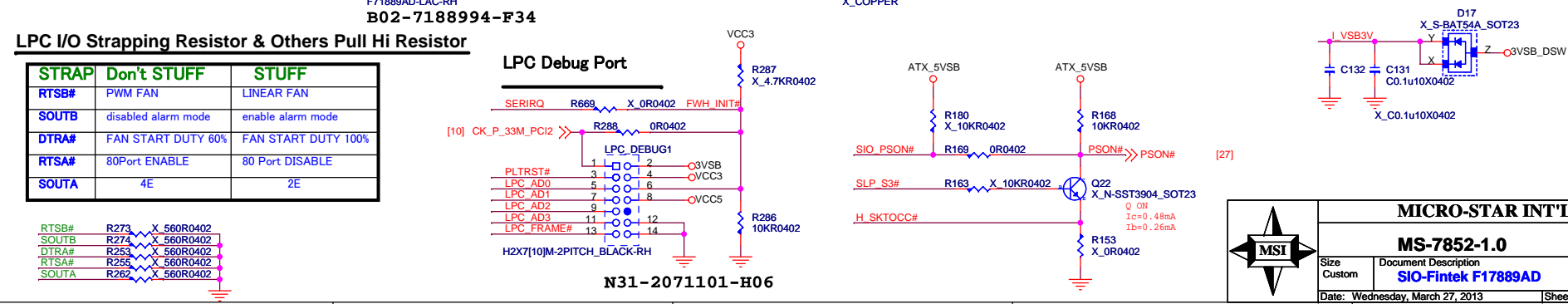
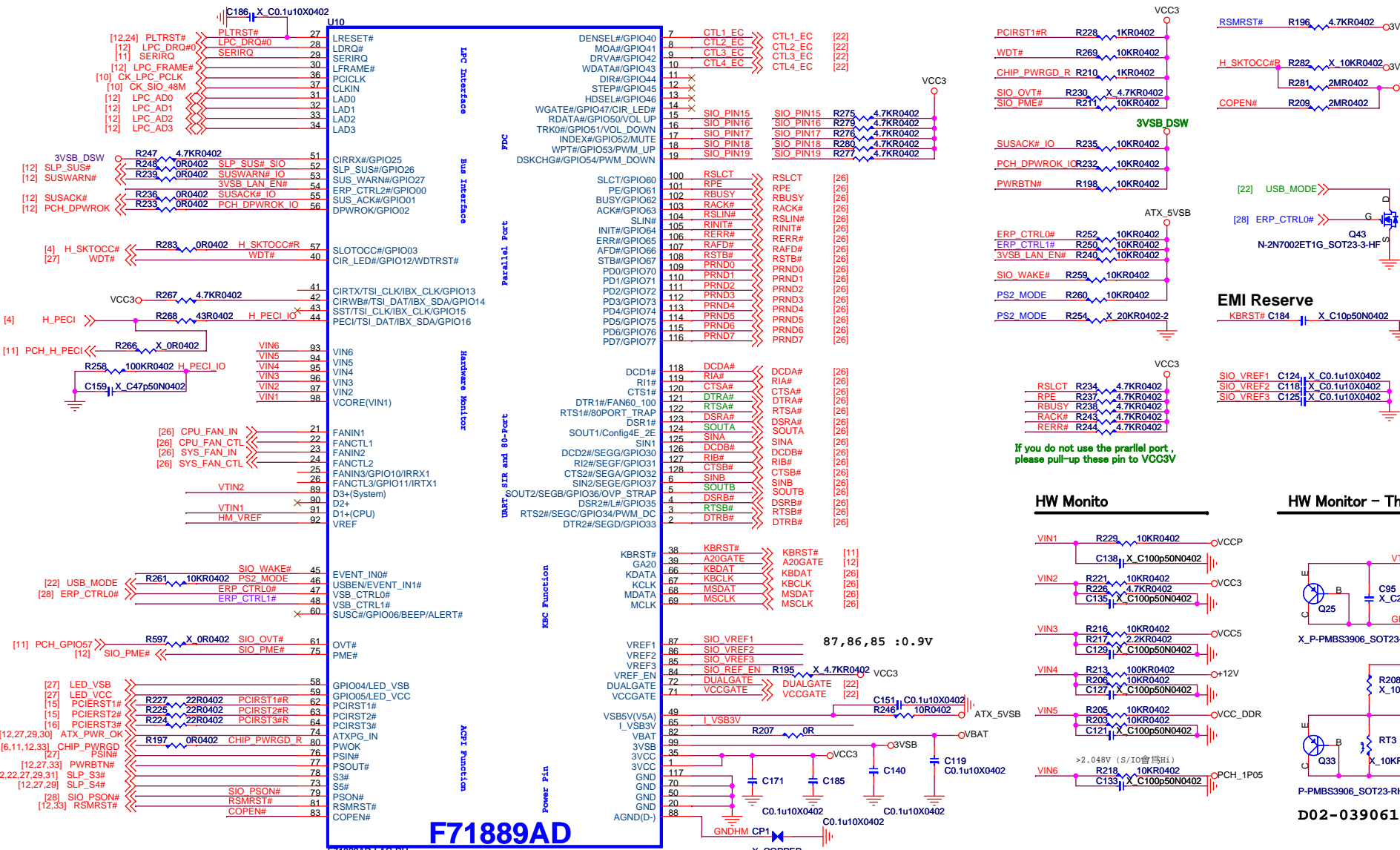
- LAN Connections:** Shows LAN\_3VSB connected to LAN\_CLK\_REQ# via R456 (10KR0402) and LAN\_PLTRST# via C406 (X\_C180p50N0402). LAN\_DISABLE# is connected to LAN\_DISABLE\_N via R437 (X\_10KR0402) and R433 (X\_10KR0402).
- SMBUS PULL-UP OPTIONS:** A text block stating: "SMBUS PULL-UP OPTIONS SMBUS SPEED (SMLINK0\_CLK and SMLINK0\_DATA) 1MHz (Default setting) 499 ohm 100KHz/400KHz 2.2K ohm".
- SMLINK0 Pull-up Details:** Two dashed green boxes show SMLINK0\_CLK and SMLINK0\_DATA each connected to a pull-up resistor (C394 and C400, X\_C10p50N0402) for EMI.

**LAN\_WAKE# connected PCH's GPIO27  
support Deep Sx Power wake on LAN**



Size Custom	Document Description <b>Gigabit LAN-Clarkville</b>	Rev <b>1.0</b>
Date: Wednesday, March 27, 2013		Sheet 24 of 40





**MICRO-STAR INT'L CO.,LTD**

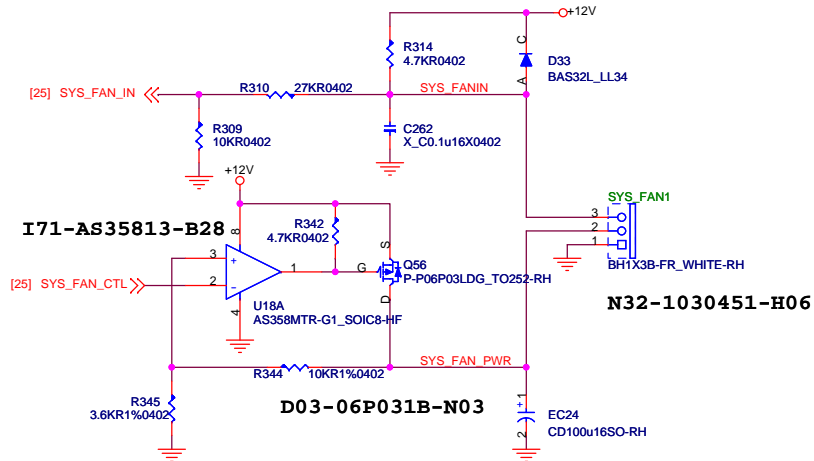
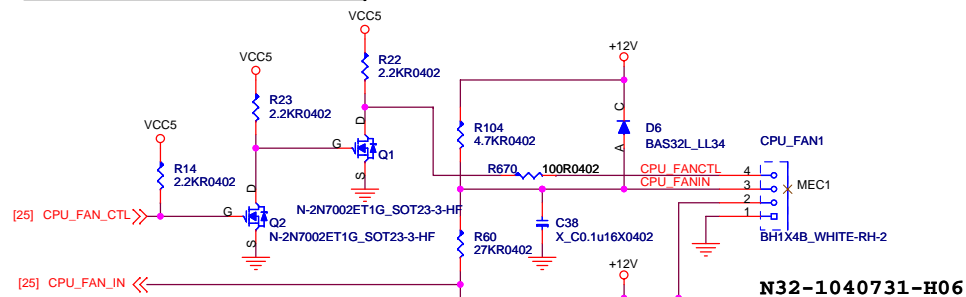
**MS-7852-1.0**

Size Custom Document Description **SIO-Fintek F71889AD** Rev **1.0**

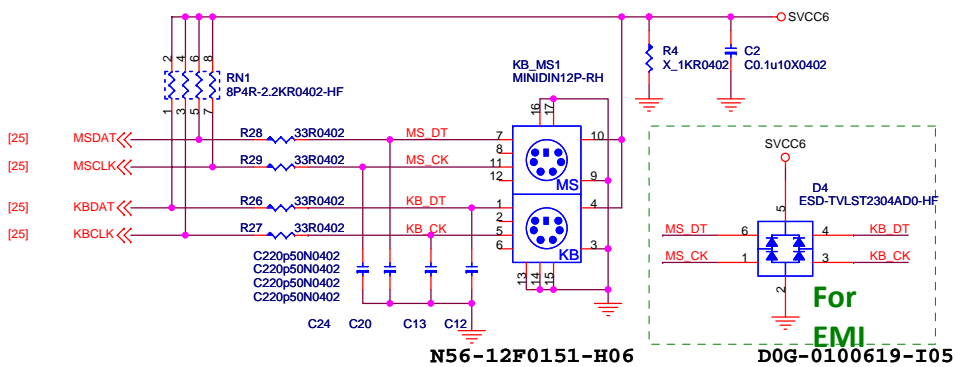
Date: Wednesday, March 27, 2013 Sheet 25 of 40



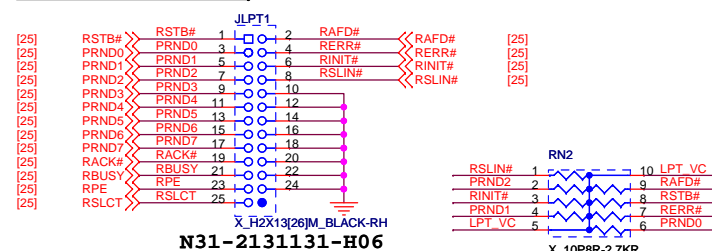
## FAN-COUNTROL CIRCUIT



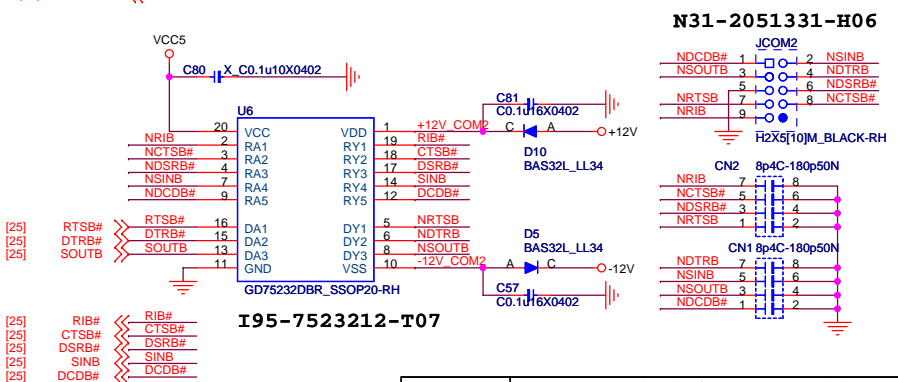
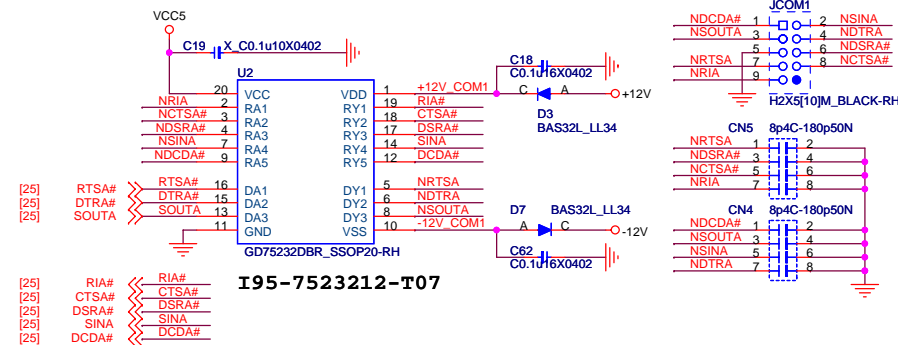
## PS2 KEYBOARD & MOUSE CONNECTOR



## Parallel Port



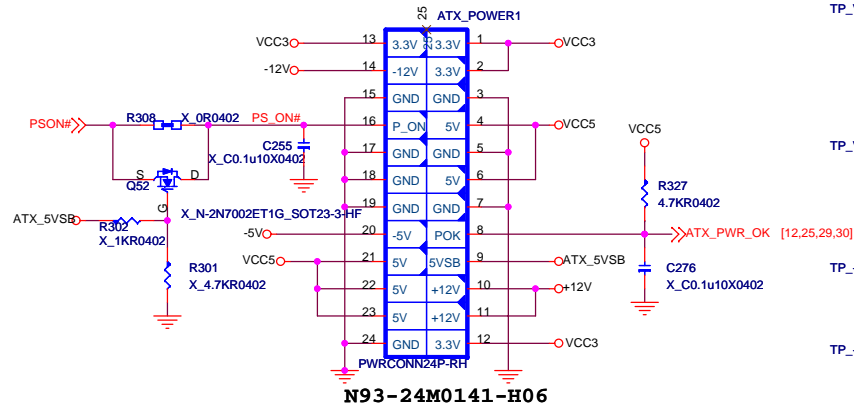
## SERIAL Port1 & Port2



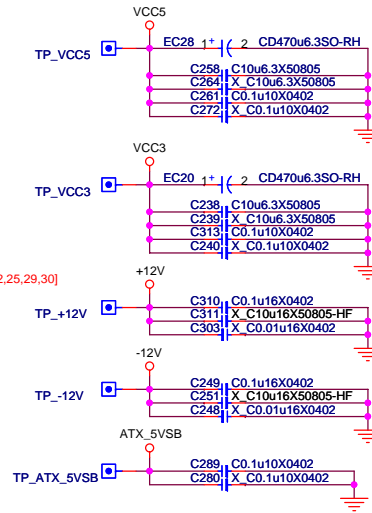
MICRO-STAR INT'L CO.,LTD		
<b>MS-7852-1.0</b>		
Size Custom	Document Description <b>FAN/PS2/COM/LPT</b>	Rev <b>1.0</b>
Date: Wednesday, March 27, 2013	Sheet 26	of 40



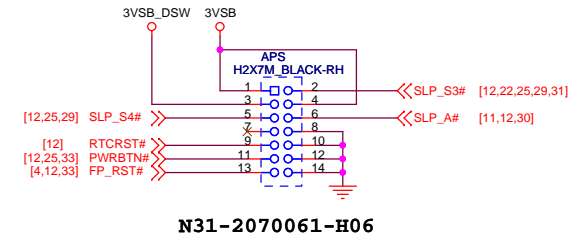
## ATX POWER CONNECTOR



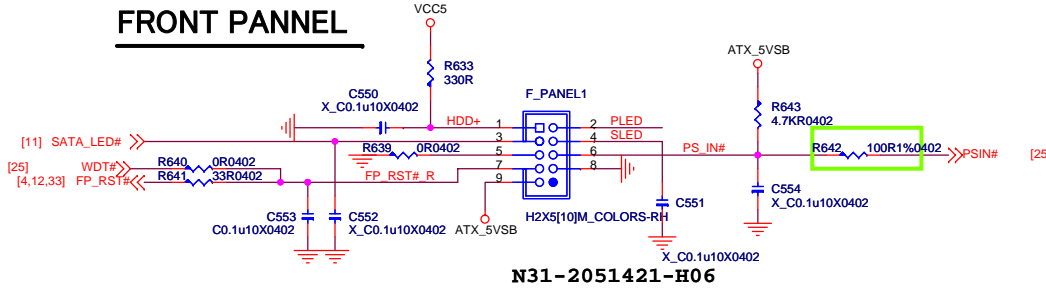
## Power Cap



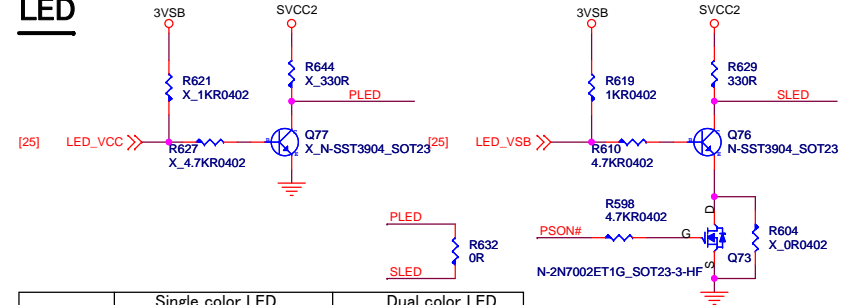
## Automatic Power Switcher (APS)



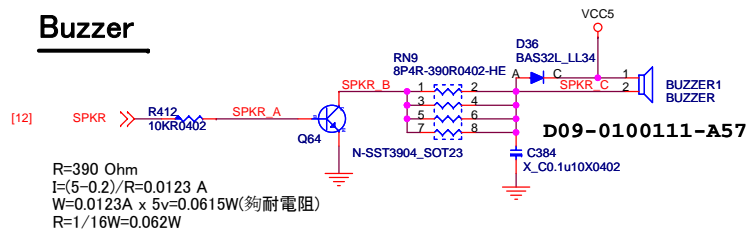
## FRONT PANNEL



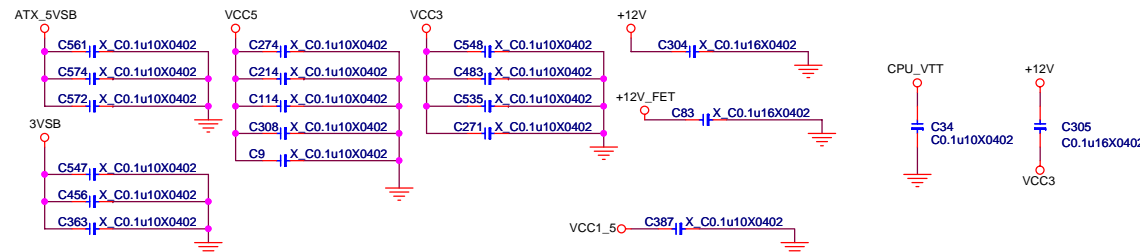
## LED



## Buzzer



## For EMI Cap



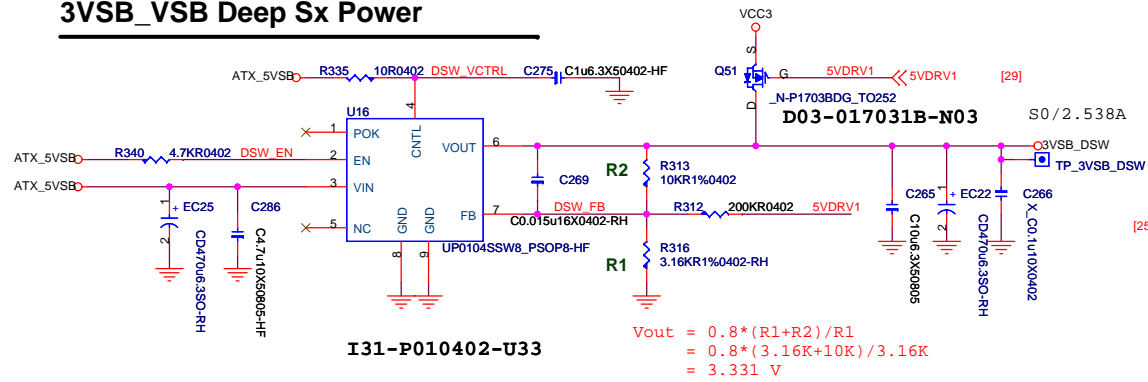
MICRO-STAR INT'L CO.,LTD

MS-7852-1.0

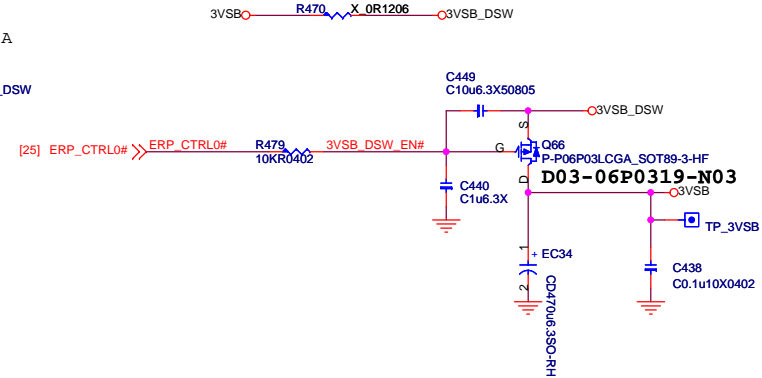
Size	Document Description	Rev
Custom	ATX PWR/FRTP/LED/Buzzer/EMI/APS	1.0
Date: Wednesday, March 27, 2013	Sheet 27 of 40	



## 3VSB\_VSB Deep Sx Power

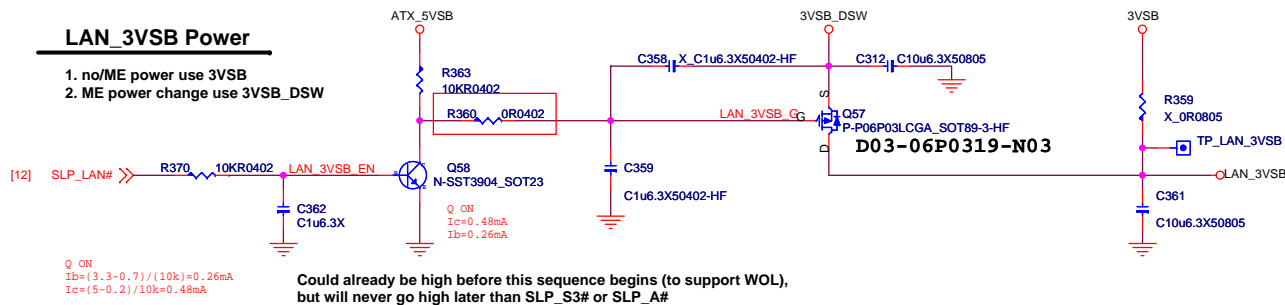


## DSW POWER CONTROL

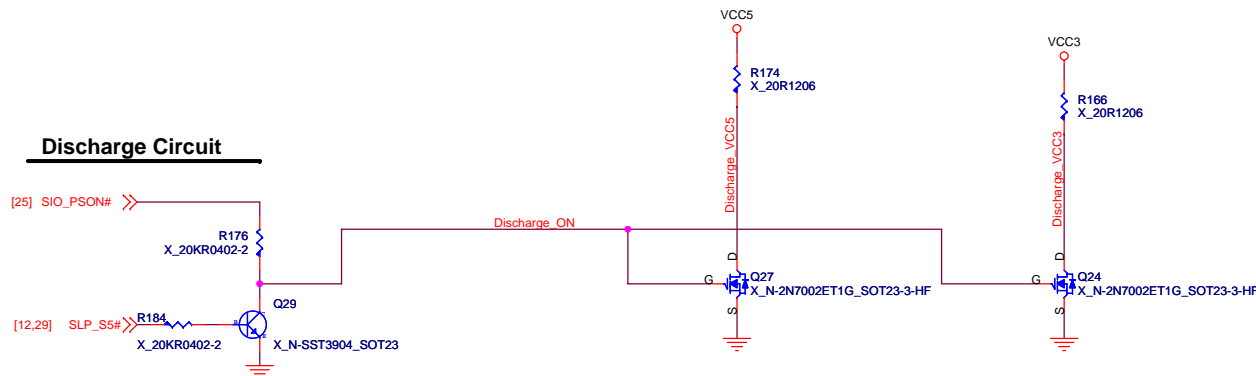


## LAN\_3VSB Power

1. no/ME power use 3VSB
2. ME power change use 3VSB\_DSW



## Discharge Circuit



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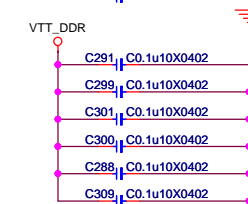
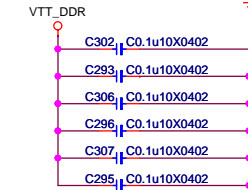
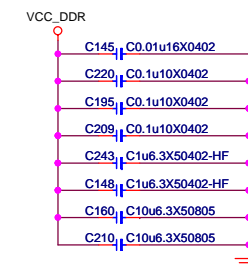
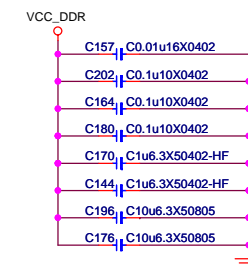
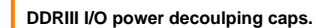
MS-7852-1.0

Size	Document Description	Rev
Custom	ACPI Controller 1	1.0
Date: Wednesday, March 27, 2013		Sheet 26 of 40

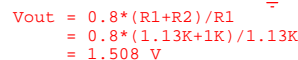


**5V - 5.8A - 29W**

Place R86 near PCH,  
near the bifurcation point of signal

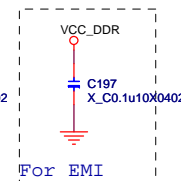
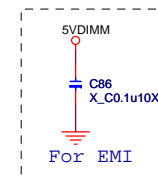


## DDRIII DIMM Power

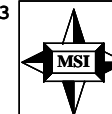


$$V_{out} = 0.8[(R_{254} + R_{246}) / R_{254}]$$

## DDRIII DIMM Power Ccntrol



Place R311 near PCH  
near the bifurcation point of signal



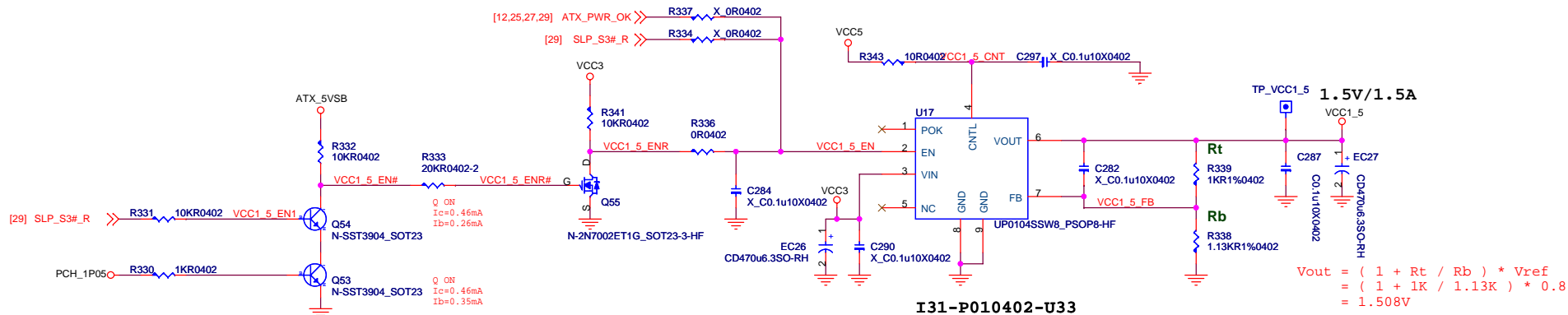
**MICRO-STAR INT'L CO.,LTD**

**MS-7852-1.0**

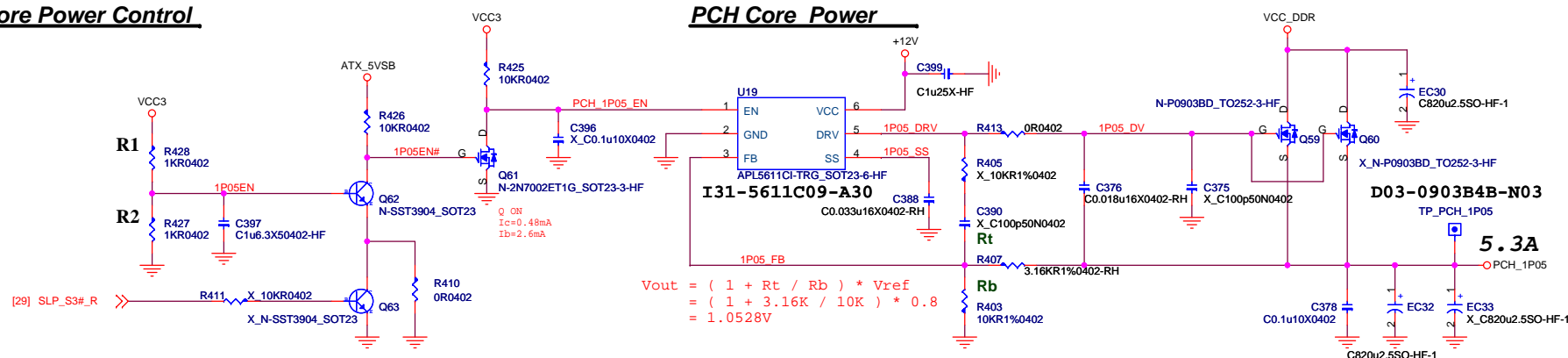
Size Custom	Document Description <b>DDR Power</b>	Rev <b>1.</b>
Date: Wednesday, March 27, 2013		Sheet 29 of 40



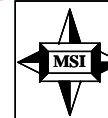
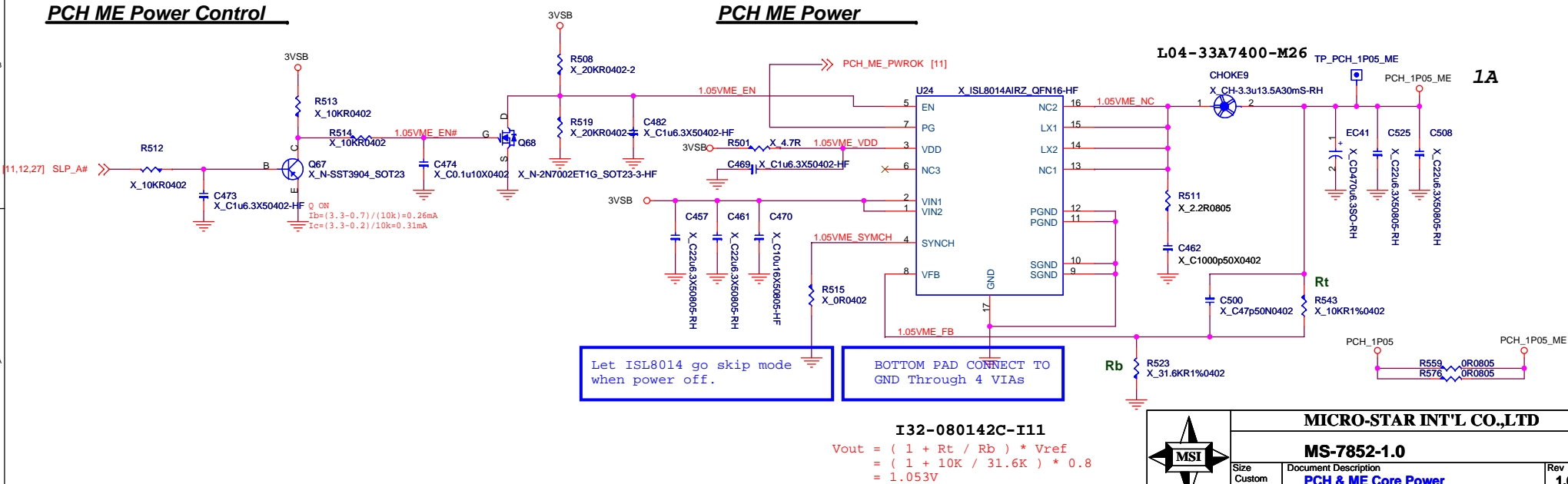
### 1.5V Power Power Control



## PCH Core Power Control



## PCH ME Power Control



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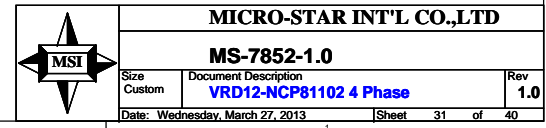
**MS-7852-1.0**

Size	Document Description
Custom	<b>PCH &amp; ME Core Power</b>

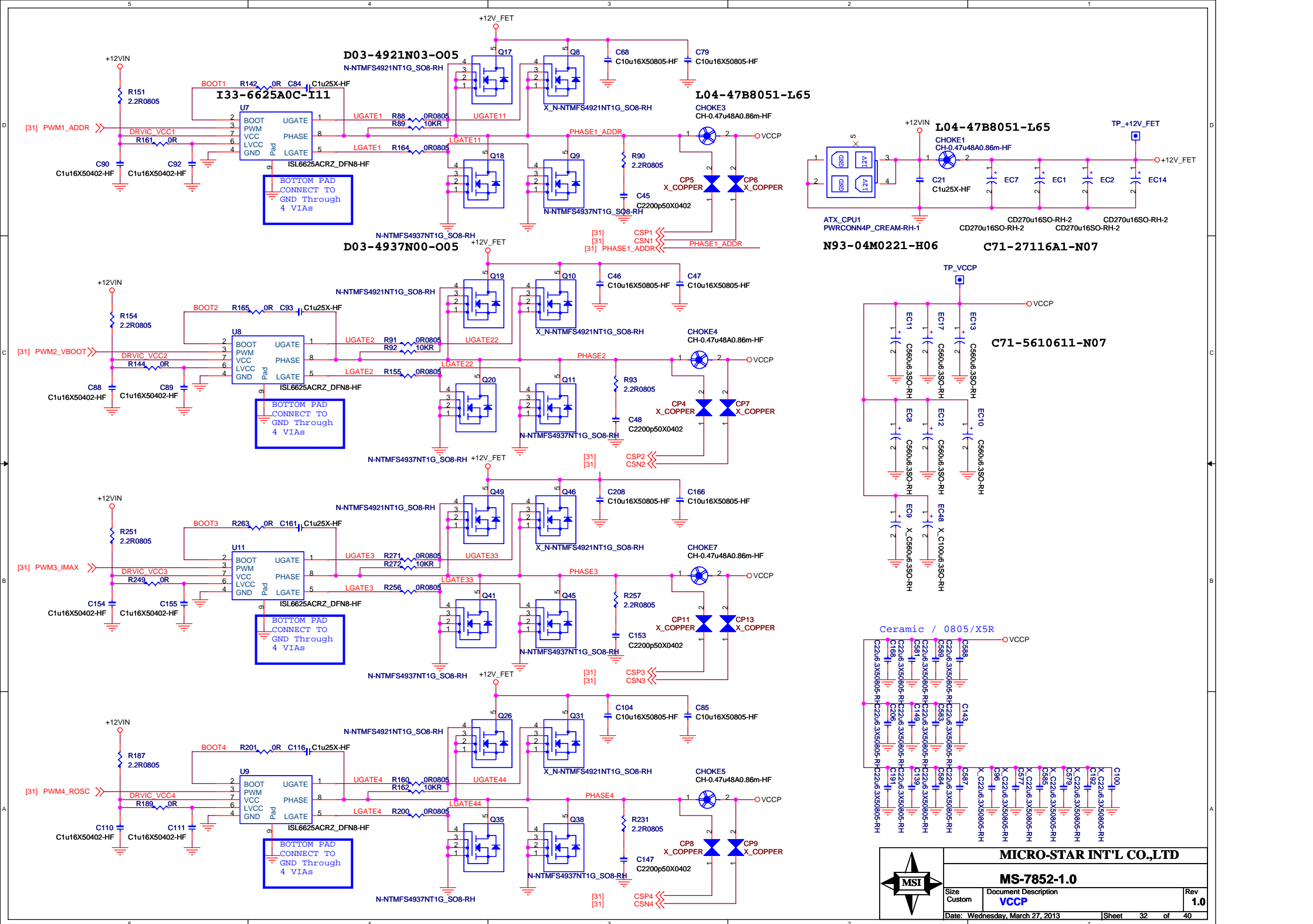
Rev	1.0
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## SharkBay VR12.5 Power Circuit - 4 Phase

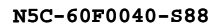








**Reserve debug port 5020**



**N5C-60F0040-S88**



## PCH XDP PWRGD/RESET



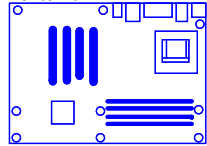
**MS-7852-1.0**

Size Custom	Document Description <b>CPU/PCH XDP</b>	Rev <b>1.0</b>
Date: Wednesday, March 27, 2013		Sheet 33 of 40



## Manual Parts

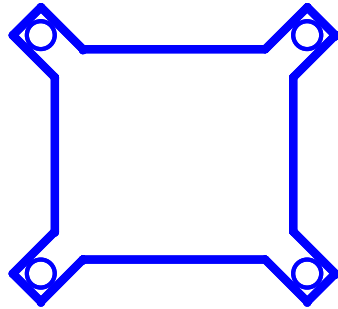
PCB1  
MS-7852-10



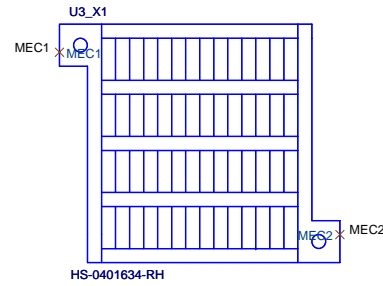
**P30-0785210-E48**

XU1\_X2

X\_CPU RETENTION BACKPLATE



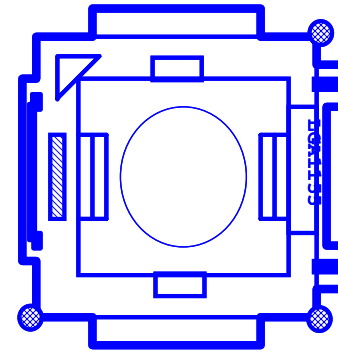
**E93-0000044-AF0**



**E31-0401634-K08**

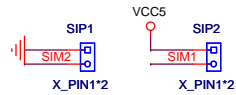
XU1\_X1

CPU SOCKET



**E21-7557060-F02**

## Simulation



VBAT-S1



BAT-BCR2032P-RH

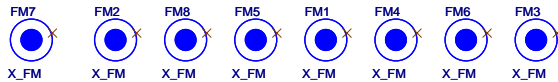
**D06-0100101-K26**



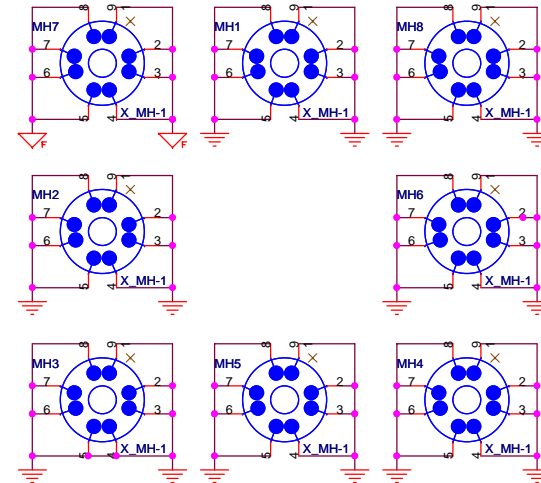
**Y01-RHDMI03-000**

## Optics Orientation Holes

Optical Fiducial Marks-120



## Mounting Holes



**MICRO-STAR INT'L CO.,LTD**

**MS-7852-1.0**

Size  
Custom

Document Description  
**Manual & Option Parts**

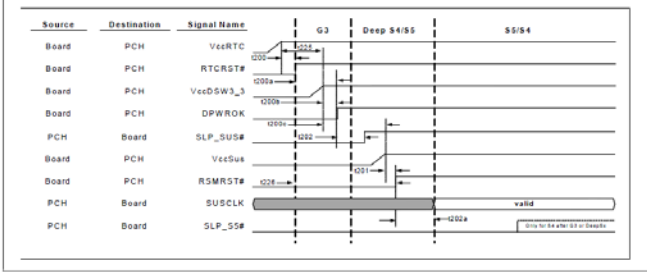
Rev  
**1.0**

Date: Wednesday, March 27, 2013

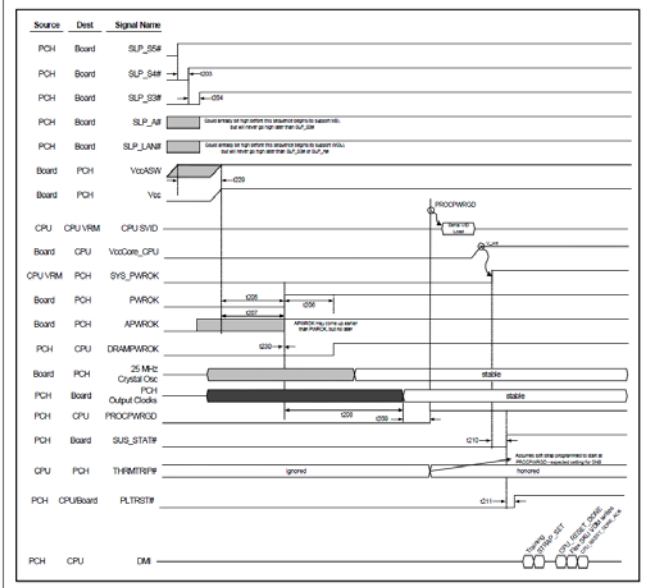
Sheet 34 of 40



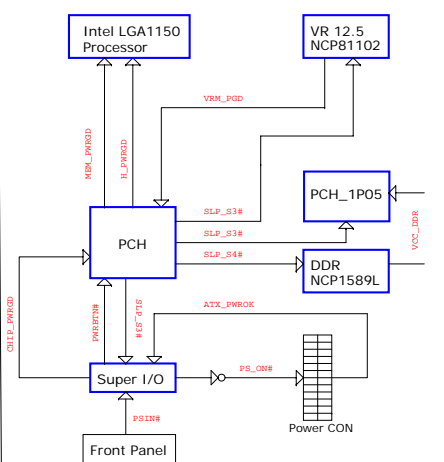
G3 w/RTC Loss to S4/S5 (With Deep Sx Support) Timing Diagram



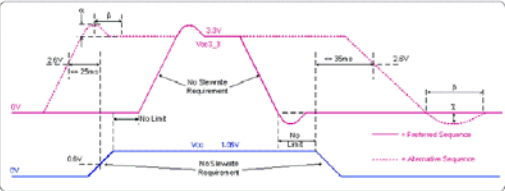
S5 to S0 Timing Diagram



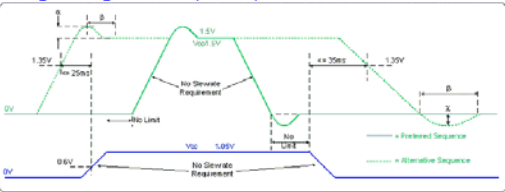
PWROK MAP



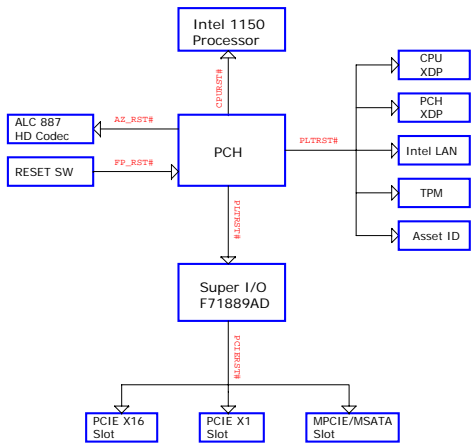
VCC3 and PCH\_1P05 Power Sequence Requirement



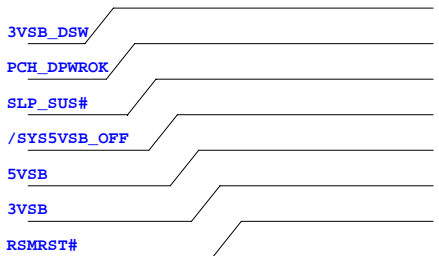
VCC1\_5 and PCH\_1P05 Power Sequence Requirement



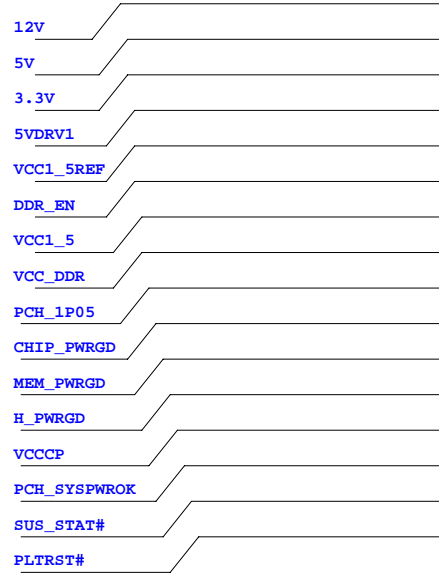
RESET MAP



G3-S5



S5-S0





ATX Power 24Pin				
12V +/-5%	3.3V +/-5%	5V +/-5%	-12V +/-5%	ATX_5VSB +/-5%

ATX 2X2Pin
+12V

PCI Express x16 Slot	
+12V	- 5.5 A
VCC3	- 3A
3VSB (wake)	- 375mA
3VSB (no wake)	- 20mA

PCI Express x1 Slot *3	
+12V	- 1.5 A
VCC3	- 9A
3VSB (wake)	- 1.125A
3VSB (no wake)	- 60mA

FAN *2	
+12V	- 0.8A

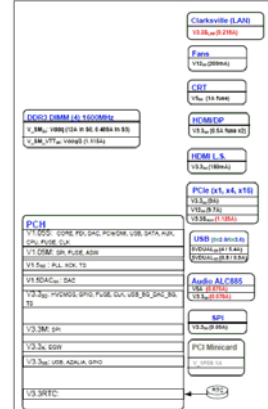
Mini PCIE, Mini SATA (2 slot)	
VCC3	- 4.4A
VCC1_5	- 1.5A

DVI	
HDMI_PWR_5V	- 180mA

VGA	
HDMI_PWR_5V	- 1A

HDMI	
HDMI_PWR_5V	- 180mA

Figure 33-2. Platform Power Map



UP7537B	USB Power	5V Linear	LAN_USB1 (USB3.0*2) SVCC4	VCC5 (S0)	- 1.8A
UP7537B	USB Power	5V Linear	ATX_5VSB (S3)	- 0.3A	
UP7537B	USB Power	5V Linear	R_USB2 (USB3.0*2) SVCC5	VCC5 (S0)	- 1.8A
UP7537B	USB Power	5V Linear	ATX_5VSB (S3)	- 0.3A	
UP7536A	USB Power	5V Linear	R_USB3 (USB2.0*2) SVCC6	VCC5 (S0)	- 1A
UP7536A	USB Power	5V Linear	ATX_5VSB (S3)	- 0.2A	
UP7536A	USB Power	5V Linear	F_USB2 (USB2.0*2) SVCC3	VCC5 (S0)	- 1A
UP7536A	USB Power	5V Linear	ATX_5VSB (S3)	- 0.3A	
UP7537B	USB Power	5V Linear	F_USBMC/R_USB2 (USB2.0*3) SVCC2	VCC5 (S0)	- 1.5A
UP7537B	USB Power	5V Linear	ATX_5VSB (S3)	- 0.3A	
UP7536A	USB Power	5V Linear	F_USB30_1 (USB3.0*1) SVCC1	VCC5 (S0)	- 0.9A
UP7536A	USB Power	5V Linear	ATX_5VSB (S3)	- 0.15A	

DUAL MOS	TP2543	5VDUAL_USB	5V Linear	F_USB30_1 CHARGE(USB3.0*1) SVCC_C	VCC5 (S0)	- 2A
					ATX_5VSB (S3)	- 7A

UP0104	3V Standby Power	3V Linear	3VSB
--------	------------------	-----------	------

Mosfet-P	3VSB_DSW	2.5A
----------	----------	------

NCP1587GD	1.5V DDR POWER	1.5V SWITCH	VCC_DDR	25A
-----------	----------------	-------------	---------	-----

UP7501	5VDUAL Power	5V Linear	5VDIMM
--------	--------------	-----------	--------

Mosfet-P	Not used	LAN_3VSB
----------	----------	----------

ISL8014	1.05 ME POWER	1.05V SWITCH	PCH_1P05_ME	Not used	1A
---------	---------------	--------------	-------------	----------	----

ISL95816HRZ	VCCP	VRD12.5	4 Phase Switch
-------------	------	---------	----------------

OP+MOS	PCH_1P05	6.3A
--------	----------	------

UP0109P	0.75V DDR POWER	0.75V linear	VTT_DDR
---------	-----------------	--------------	---------

Haswell CPU Intel LGA 1150	
VCCP	- 70A
VCC_DDR	- 4.2A
PCH_1P05	- 300mA

Lynx Point PCH	
PCH_1P05	- 5A
VCCCORE   VCCIO   VCCCLK	- 1A
VCCSSC   VCCUSBPLL	- 0.25A
VCCSW	- 188mA
VCC3_3   VCCCLK3_3	- 22mA
LAN_3VSB	- 261mA
VCCSPI	- 15mA
3VSB_DSW	- 6uA
VBAT	- 6uA

SIO F71889AD	
VCC3	- 10mA
VCC   AVCC	- 8mA
3VSB_DSW	- 1uA
VBAT0	- 1uA

DIMM (2 Channel / 2 Per Channel)	
VCC_DDR	- 12A
VDD	- 1.1A
VTT_DDR	- 1.1A

LAN-Clarkville	
LAN_3VSB	- 132mA
AVDD33   DVDD33	- 500mA
V_1P0_LAN	- 500mA
AVDD10   DVDD10	- 500mA

AUDIO ALC887-VD	
ATX_5VSB	- 52mA
LDO-IN	- 12mA
VCC3	- 5mA
DVDD   DVDD-IO	- 20mA

Internal Switch
-----------------

CPU_VTT
---------

3V Battery
------------

Internal Switch
-----------------

V_1P0_LAN
-----------



## Intel Lynx Point GPIO

Name	Net Name	Power Well	Default	NOTES
GPIO00	BM_BUSY#	Core	GPI	not use pull up VCC3
GPIO01	PCH_GPIO1	Core	GPI	not use pull up VCC3
GPIO02	SPI_WP#_PCH	Core	GPI	MB_ID / pull up VCC3
GPIO03	MB_ID3	Core	GPI	MB_ID / pull up VCC3
GPIO04	MB_ID2	Core	GPI	MB_ID / pull up VCC3
GPIO05	MB_ID1	Core	GPI	not use pull up VCC3
GPIO06	PCH_GPIO6	Core	GPI	not use pull up VCC3
GPIO07	PCH_GPIO7	Core	GPI	not use pull up VCC3
GPIO08	PCH_GPIO8	Suspend	GPO	not use
GPIO09	USB_OCP#5	Suspend	Native	not use pull up 3VSB / PCH XDP port
GPIO10	USB_OCP#6	Suspend	Native	not use pull up 3VSB / PCH XDP port
GPIO11	PCH_SMBALERT#	Suspend	Native	not use pull up 3VSB
GPIO12	LAN_DISABLE#	DSW	Native	LAN_DISABLE# function Low Disable LAN chip
GPIO13	PCH_GPIO13	Suspend	GPI	SIO_OVT# function Low Active / pull up 3VSB
GPIO14	USB_OCP#7	Suspend	Native	not use pull up 3VSB / PCH XDP port
GPIO15	MINI_PWRON	Suspend	GPO	MINI_PWRON function pull up 3VSB
GPIO16	PCH_GPIO16	Core	GPI	not use internal pull-up / PCH XDP port
GPIO17	PCH_GPIO17	Core	GPI	not use pull up VCC3
GPIO18	PCH_GPIO18	Core	Native	not use pull up VCC3 / PCH XDP port
GPIO19	PCH_GPIO19	Core	GPI	BIOS LPC SPI Strapping pull up VCC3 / PCH XDP
GPIO20	PCH_GPIO20	Core	Native	not use pull up VCC3 / PCH XDP port
GPIO21	MSATA_DET	Core	GPI	MSATA_Detect function pull up VCC3
GPIO22	PCH_GPIO22	Core	GPI	not use pull up VCC3
GPIO23	LPC_DRQ1#	Core	Native	not use / internal pull-up
GPIO24	PCH_GPIO24	Suspend	GPO	not use pull up 3VSB
GPIO25	PCH_GPIO25	Suspend	Native	not use pull up 3VSB
GPIO26	MINI_CLKREQ#	Suspend	Native	pull up 3VSB
GPIO27	LAN_WAKE#	DSW	GPI	LAN_WAKE# function pull up 3VSB_DSW
GPIO28	PCH_GPIO28	Suspend	GPO	not use pull up 3VSB
GPIO29	SLP_WLAN#	DSW	Native	SLP_WLAN# pull up 3VSB_DSW
GPIO30	SUSWARN#	Suspend	Native	SUSWARN# function
GPIO31	PCH_GPIO31	DSW	GPI	not use pull up 3VSB_DSW
GPIO32	PCH_GPIO32	Core	GPO	not use pull up VCC3
GPIO33	SPI_HOLD_GPO#	Core	GPO	pull up VCC3 / SPI_HOLD_GPO# Active Low
GPIO34	STP_PCI#	Core	GPI	not use pull up VCC3
GPIO35	PCH_GPIO35	Core	GPO	not use pull up VCC3 / PCH XDP port
GPIO36	PCH_GPIO36	Core	GPI	not use internal pull-up / PCH XDP port
GPIO37	PCH_GPIO37	Core	GPI	not use pull up VCC3 / PCH XDP port
GPIO38	PCH_GPIO38	Core	GPI	not use pull up VCC3 / PCH XDP port
GPIO39	PCH_GPIO39	Core	GPI	not use pull up VCC3
GPIO40	USB_OCP#1	Suspend	Native	not use pull up 3VSB / PCH XDP port
GPIO41	USB_OCP#2	Suspend	Native	not use pull up 3VSB / PCH XDP port
GPIO42	USB_OCP#3	Suspend	Native	not use pull up 3VSB / PCH XDP port
GPIO43	USB_OCP#4	Suspend	Native	not use pull up 3VSB / PCH XDP port
GPIO44	LAN_CLKREQ#	Suspend	Native	pull up 3VSB
GPIO45	PCH_GPIO45	Suspend	Native	not use pull up 3VSB
GPIO46	ME_CTL	Suspend	Native	ME lock pull up 3VSB
GPIO47	NA	Suspend	Native	NA
GPIO48	PCH_GPIO48	Core	GPI	not use pull up VCC3
GPIO49	PCH_GPIO49	Core	GPI	not use pull up VCC3 / PCH XDP port
GPIO50	MB_ID0	Core	GPI	MB_ID / pull up VCC3
GPIO51	PCH_GPIO51	Core	GPO	BIOS LPC SPI Strapping / internal pull-up
GPIO52	PCH_GPIO52	Core	GPI	not use pull up VCC3
GPIO53	PCH_GPIO53	Core	GPO	not use
GPIO54	PCH_GPIO54	Core	GPI	not use pull up VCC3
GPIO55	PCH_GPIO55	Core	GPO	not use
GPIO56	NA	Suspend	Native	NA
GPIO57	PCH_GPIO57	Suspend	GPI	not use pull up 3VSB
GPIO58	SMLINK1_CLK	Suspend	Native	not use pull up 3VSB
GPIO59	USB_OCP#0	Suspend	Native	not use pull up 3VSB / PCH XDP port
GPIO60	PCH_SML0ALERT#	Suspend	Native	not use pull up 3VSB
GPIO61	PCH_GPIO61	Suspend	Native	not use pull up 3VSB
GPIO62	SUS_CLK	Suspend	Native	not use / No external resistors required
GPIO63	SLP_S5#	Suspend	Native	No pull up/down resistors needed
GPIO64	Open	Core	Native	not use
GPIO65	Open	Core	Native	not use
GPIO66	Open	Core	Native	not use

## Intel Lynx Point GPIO

Name	Net Name	Power Well	Default	NOTES
GPIO67	CK_SIO48M	Core	Native	SIO_48M_clock
GPIO68	EXP_PRSTNT2#	Core	GPI	PCIE_16X PRSTNT2 pull up VCC3
GPIO69	PCH_GPIO69	Core	GPI	not use pull up VCC3
GPIO70	MSATA_EN	Core	Native	MSATA_EN function pull up VCC3
GPIO71	PCH_GPIO71	Core	Native	not use pull up VCC3
GPIO72	PCH_GPIO72	DSW	Native	not use pull up 3VSB_DSW
GPIO73	PCH_GPIO73	Suspend	Native	not use pull up 3VSB
GPIO74	PCH_SMLIALERT#	Suspend	Native	not use pull up 3VSB
GPIO75	SMLINK1_DATA	Suspend	Native	not use pull up 3VSB

## Fintek F71889AD GPIO

Name	Net Name	Number	Power Well	NOTES
GPIO00	3VSB_LAN_EN#	54	I_VSB3V	Not used pull up ATX_5VSB
GPIO01	SUSACK#_SIO	55	I_VSB3V	SUSACK#
GPIO02	DPWROK_SIO	56	VBAT	DPWROK
GPIO03	H_SKTOCC#_R	57	I_VSB3V	CPU socket SKTOCC#_R
GPIO04	LED_VSB	58	I_VSB3V	LED_VSB
GPIO05	LED_VCC	59	I_VSB3V	LED_VCC
GPIO06	Open	60	I_VSB3V	NC
GPIO10	Open	25	VCC	NC
GPIO11	Open	26	VCC	NC
GPIO12	WDT#	40	VCC	WDT# (Front reset FP_RST#)
GPIO13	Open	41	VCC	NC
GPIO14	N241479349	42	VCC	Not used pull up VCC3
GPIO15	Open	43	VCC	NC
GPIO16	PECI_IO	44	VCC	PECI
GPIO25	N162193265	51	I_VSB3V	Not used pull up 3VSB_DSW
GPIO26	SLP_SUS#_SIO	52	I_VSB3V	SLP_SUS#
GPIO27	SUSWARN#_SIO	53	I_VSB3V	SUSWARN#
GPIO30	DCDB#	126	VCC	DCDB#
GPIO31	RIB#	127	VCC	RIB#
GPIO32	CTSB#	128	VCC	CTSB#
GPIO33	DTRB#	2	VCC	DTRB#
GPIO34	RTSB#	3	VCC	RTSB#
GPIO35	DSRB#	4	VCC	DSRB#
GPIO36	SOUTB	5	VCC	SOUTB
GPIO37	SINB	6	VCC	SINB
GPIO40	CTL1_EC	7	I_VSB3V	Control iCharge states
GPIO41	CTL2_EC	8	I_VSB3V	Control iCharge states
GPIO42	CTL3_EC	9	I_VSB3V	Control iCharge states
GPIO43	Open	10	I_VSB3V	NC
GPIO44	Open	11	I_VSB3V	NC
GPIO45	Open	12	I_VSB3V	NC
GPIO46	Open	13	I_VSB3V	NC
GPIO47	Open	14	I_VSB3V	NC
GPIO50	SIO_PIN15	15	I_VSB3V	Not used pull up VCC3
GPIO51	SIO_PIN16	16	I_VSB3V	Not used pull up VCC3
GPIO52	SIO_PIN17	17	I_VSB3V	Not used pull up VCC3
GPIO53	SIO_PIN18	18	I_VSB3V	Not used pull up VCC3
GPIO54	SIO_PIN19	19	I_VSB3V	Not used pull up VCC3
GPIO60	RSLECT	100	VCC	Not used pull up VCC3
GPIO61	RPE	101	VCC	Not used pull up VCC3
GPIO62	RBUSY	102	VCC	Not used pull up VCC3
GPIO63	RACK#	103	VCC	Not used pull up VCC3
GPIO64	RINIT#	105	VCC	NC
GPIO65	RERR#	106	VCC	Not used pull up VCC3
GPIO66	RAFD#	107	VCC	NC
GPIO67	RSTB#	108	VCC	NC
GPIO70	PRND0	109	VCC	NC
GPIO71	PRND1	110	VCC	NC
GPIO72	PRND2	111	VCC	NC
GPIO73	PRND3	112	VCC	NC
GPIO74	PRND4	113	VCC	NC
GPIO75	PRND5	114	VCC	NC
GPIO76	PRND6	115	VCC	NC
GPIO77	PRND7	116	VCC	NC



MS-7852 Revision History List

Ver.	DATE	Schematic Change List	
0A	2012.9.28	7852-0A Gerber out.	
	2012.10.3	BOM: 601-7852-A10	Page. 34
	2012.10.9	SCH: Add HDMI VIRTUAL Y01-RHDMI03-000 BOM: Reaktek suggestion add R577, R595 R11-0223012-W08 BOM: Add R469, R476 R11-0103012-W08 BOM: ESD parts D0G-0100619-I05 add AVLDOG-0200529-A68	Page. 23 Page. 12
	2012.10.19 2012.12.07	BOM: EC10,EC11,EC12,EC13,EC17,EC8,EC9 change use C71-5610611-N07 BOM: AVL by byer request	Page. 32
0B	2012.11.09	SCH: circuit error, USBP10 change to U26.10pin, USBN10 change to U26.11pin. SCH: R170 change connect to Q32 1pin and 4pin SCH: circuit error, JCOM2 change 2pin-NSINB / 4pin-NDTRB / 7pin-NRTSB / 9pin-NRIB SCH: Realtek change. U25.38pin add C602 10uF SCH: Buyer request VGA_DVI1A change use N58-39F0221-K06, (footprint IOASM_VGA15_DVI24_9) SCH: MSATA1 VCC3 add C604, C605, C606 0.1uF and VCC1_5 add C607 0.1uF SCH: customer request reserve U33, C603 for PCIE16X PCIERST1# and PCH_GPIO13 reset function. and R352 BOM add 0Rohm SCH: SIO_OVT change connect to PCH_GPIO57, R597 footprint change. VRM Power solution SCH: Q8, Q9, Q10, Q11, Q17, Q18, Q19, Q20, Q26, Q31, Q35, Q38, Q41, Q45, Q46, Q49 footprint change use SOT669_COLAY BOM: CHOKE1, CHOKE3, CHOKE4, CHOKE5, CHOKE7 change use L04-47B8051-L65 BOM: Remove EC9, Q8, Q10, Q31, Q46 BOM: Change R102 use 3.4Kohm, R97 use 115Kohm, R12 use 51Kohm, R86 use 1.21Kohm, SCH: U1.15pin add R661 4.7Mohm to GND, C40 change C820p50X0402 VCC_DDR Power solution SCH: Choke change use L04-05A7341-L65 (footpirt CHK_D2_10_3X6_3_1) BOM: Change R45 use 3.16Kohm, R120 use 8.2Kohm. BOM: Doc #489996 note 1.3.2 --> VCC_DDR power 9pcs change use 4pce 0805, 22 uF at the CPU side. remove C187, C201, C207, C217, C231 Other power SCH: Power team and buyer suggestion U16 and U17 change use I31-P010402-U33 BOM: R36 change use 110ohm and R40 remove follow CRB BOM: SATA4_GP R378 remove and R388 add 10Kohm BOM: remove EC33, add EC32	Page. 22 Page. 29 Page. 26 Page. 23 Page. 19  Page. 16 Page. 15  Page. 25  Page. 31, 32       Page. 29  Page. 6  Page. 28, 30 Page. 31 Page. 11 Page. 30 Page. 27 Page. 12  Page. 29  Page. 13  Page. 30 Page. 28 Page. 16 Page. 28 Page. 24, 2
	2012.11.20	SCH: customer request add APS CON (Automatic Power Switcher) SCH: customer request ME luck circuit change resvered ME_LOCK1 Jump / change: R649, R650 / add: Q79, JQ80, R662, R663, R664 BOM: Power-on VCC5 droop issue, adjusted 5VDR1 rise time the R116 change use 10K (R11-0103033-R01) Improve VCC5 droop. BOM: PCH_IP05_overshoot_143mV, remove R405, C390, change R413=0R0402, C388=0.033uF, C376=0.018uF BOM: PCH_IP05_R403=10K1%0402, R407=3.16K1%0402 BOM: VCCADAC too low, R490 change use 0ohm R11-0000013-W08 BOM: VCC3 voltage too high, R313 change us 10K1%0402, R316 change use 3.16K1%0402 SCH: Wifi CARD VCC3 leakage issue, reserve D47, BOM remove R440 BOM: PSON# voltage difference. remove Q24, Q27, Q29, R166, R174, R176, R184 SCH: LAN SMLINK0_CLK and SMLINK0_DATA add R665 and R666 499ohm1%0402 pull-high LAN_3VSB. BOM remove R574 and R589 BOM: LAN power source change use 3VSB_DSB for BIOS LAN power ON/OFF function Remove R359, Add Q57, Q58, R370=R363=10K0402, R360=0ohm0402, C362 1u6.3X, C359 1u6.3X50402 BOM: LAN_WAKE# pull-high R587 change use 4.7K0402	Page. 28 Page. 31 Page. 11 Page. 30 Page. 27 Page. 12  Page. 29  Page. 13  Page. 30 Page. 28 Page. 16 Page. 28 Page. 24, 2  Page. 28  Page. 11

Ver.	DATE	Schematic Change List	
0B		BOM: U21_BIOS change use W25Q64FVSSIQ ( M31-25Q6443-W03 )	Page. 12
	2012.12.18	7852-0B Gerber out.	
	2013.1.10	VRM Power solution BOM: Add C60 = C1000p50N0402-HF / C11-1021812-M09 . R101= 3.32KR1%0402 / R11-3321T12-W08 R54, R61, R79, R55, R58, R76 = 10KR1%0402 / R11-0103T12-W08 R97 change use 105KR1%0402 / R11-1053T12-W08 BOM: ME_LOCK1 issue remove Q79 BOM: LAN_3VSB regulator power source 3VSB_DSW add C312 C10u6.3X50805	Page. 31  Page. 12 Page. 28
	2013.2.25	SCH: ME_LOCK1 circuit error the modify Q79 and BOM add Q79 SCH: SPI1 circuit error the modify Q65 and SPI_CS0_F# add pull-high R667 2.2Kohm SCH: F_PANEL1 pin6 to PS_IN# and pin8 to GND SCH: TP2543 ILIM_SEL reserved R668 SIO GPIO43, net CTL4_EC_R. BOM: HDMI SA quality R171, R173, R175, R179, R181, R183, R185, R188 change use 470ohm (reference Intel doc. #489996 1.3.2) BOM: VRM light loading, R97 change use 102KE1%0402 / R11-1023T12-W08 SCH: SMB reserved parts C608, C609, C610, D48 for EMI and ESD in PCIE slot SCH: SPI ROM library and footprint change SCH: F_USB30_1 modify library for N32-2101211-H06, footprint change use BHEAD2X10_2MM_NP20_TEST (N32-1901231-H06 and N32-2101211-H06 library pin define are difference)	Page. 12  Page. 27 Page. 22 Page. 18  Page. 31 Page. 15 Page. 12 Page. 20  Page. 33 Page. 26 Page. 25  Page. 26 Page. 20
10	2013.3.5	SCH: Q56 change use D03-06P031B-N03 SCH: LPC_DEBUG1 footprint change use BHEAD2X7_2MM_NP10, 2nd pin link to 3VSB and 6th pin reserved R669 link to net SERIRQ for debug port SCH: CPU_FANCTL add R670 100R0402 for ESD SCH: D38 change use D0G-05A0300-I14 by customer request.	Page. 24, 21  Page. 12 Page.
	2013.3.11	SCH: JXDP1 and JXDP2 footprint change (Mask), BOM remove JXDP1	
	2013.3.15	SCH: Q56 change use D03-06P031B-N03	
	2013.3.19	SCH: LPC_DEBUG1 footprint change use BHEAD2X7_2MM_NP10, 2nd pin link to 3VSB and 6th pin reserved R669 link to net SERIRQ for debug port SCH: CPU_FANCTL add R670 100R0402 for ESD SCH: D38 change use D0G-05A0300-I14 by customer request.	
	2013.3.26	SCH: D38 change use D0G-05A0300-I14 by customer request.	
	2013.3.27	7852-0B Gerber out. BOM: LAN_USB1 change use N58-32F0101-F02 (buyer and PM request). USB weak to plug out force too low, custmoer SPEC 0.8kg BOM: SPI ROM socket U21 remove, U21_BIOS change to 5010	

MS-7852 BOM List

Schematic Cfg	ERP NO.	Remark
Cfg 7852-0A-H87	601-7852-A10	H87
Cfg 7852-0B-H87	601-7852-B10	
Cfg 7852-10-H87		



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